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Report

High Temperature Power Electronics Packaging

Reliable packaging technologies for high temperature applications

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ABSTRACT

Reliable packaging technologies for high temperature applications

The lack of robust and reliable packaging methods are considered to be one of the main challenges for the next generation of high temperature electronics (>200 °C). Power electronics are especially difficult to operate in this environment. This project investigated packaging technologies suitable for a high temperature power module for operation up to 250 °C. The key technologies investigated were:

- A novel type ceramic substrate active metal brazed (AMB) silicon nitride (Si_3N_4) showed no signs of degradation.
- A state-of-the-art Au-Sn solid-liquid interdiffusion (SLID) die attach was developed.
- Silicon carbide reinforced aluminium (AlSiC) with cold sprayed Cu was used as a base plate.
- Different thermal interface materials were investigated.
- Finally, a power module concept was developed. It was based on silicon carbide (SiC) bipolar transistors (BJT).

The main conclusion drawn from this project is that reliable packaging technologies for 200 °C and beyond seem possible. Suitable packaging technologies are emerging but commercially available electronic components compatible with this temperature range and these novel technologies are still very sparse.

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APPENDICES

1 Summary

The need for electronics which will operate reliably at high temperature is continuously increasing in the world in general, and especially in the Norwegian oil industry and its associated service companies.

There are mainly two reasons for this:

- The petroleum wells go deeper and the environmental temperature increases
- Several novel drilling- and data collection technologies are based on electrical power

This has led to a need for power control for motors in the kW range operating past 200 °C

There is also a continuous search for new methods in oil exploration. Many of these are based on high temperature electronics. Several of our industrial partners have expressed these reasons for their interest in contributing to the project.

In a greater picture, a strong market pull for high temperature electronics also comes from the aerospace and the automotive industry. Interesting enough, the new "green technologies" like electrical cars and geothermal energy are also in need for electronic power control and very high temperature operations.

Electronic control of high power at high environmental temperatures is a multidisciplinary activity. Just as important as the temperature rating of the individual components is their packaging. Here compactness must be blended with efficient heat transport, mechanical robustness and good electrical performance.

And further on; the properties of the materials used are not limited to strength, heat conductivity and electrical insulation. Their mutual chemical, mechanical and electrical interference is just as important in obtaining a high performance reliable result.

This background is reflected in the objectives and the working methods chosen for the High Temperature Power Electronics Packaging (HTPEP) project.

The primary objective was:
Develop reliable packaging technology for power electronic systems operating at temperatures up to 250 °C.

This was broken down into a number of secondary objectives:

- Develop processes for packaging of SiC and passive components for HT-applications.
- Improve knowledge on failure mechanisms occurring in interconnects and materials used
- Build know-how on SiC component technology

In order to come close to the real world problems that would meet a designer of high power, high temperature electronics, we decided to develop a demonstrator as a part of the project. In cooperation with our industrial partners we chose to make a SiC-power switch for motor control in the kW region.

The main scientific contributions and lessons learned during the project are listed below:

- The foremost achievement for this project was the development of a high temperature (>250 °C) die attach technology; *Au-Sn Solid Liquid Inter-Diffusion (SLID) bond process*. It has proven to be state-of-art and is by far, as far as the authors know, the most robust and reliable joining technology for harsh applications there is. It was mainly developed within the frame of the PhD study with great synergy and support from the project.
- The emerging ceramic substrate technology based on silicon nitride with active metal brazed (AMB) Cu conductors was shown to be thermo-mechanically robust and a fine match to the silicon carbide (SiC) components for operation up to 250 °C. Plating a patterned substrate with the correct metallization (Cu / Ni / Au) proved to be troublesome, but not restrictive. It will, however, require some effort to develop it into an efficient industrial process.
- Strength evaluation of solid joints must be performed at the operation temperature to provide trustworthy information. This discovery will be provided as a suggestion for improvement of future revisions of international standards, e.g. MIL-STD-883.

- Au wire bonds to Au pads were evaluated and qualified as reliable high temperature interconnects (up to 250 °C).
- Design rules for the application of high temperature compatible ceramic circuit boards were developed.
- Know-how on bipolar junction (BJT) SiC transistors was developed.
- Know-how on feasible high temperature materials such as structural components, thermal interface materials (TIM) and conformal coatings was developed.

We also experienced that:

- High temperature electronic components, especially capacitors and more advanced circuits (e.g. microcontrollers and memory) are still extremely sparse, limiting the freedom of choice for electrical designs for 250 °C specification. But there is a tremendous R&D activity around the globe nowadays.
- *Bare die* components with custom made metallization schemes are very hard to get from commercial companies. (I.e. Au based systems instead of the more common and traditional but inadequate Al schemes.) For reliable high temperature system solutions this is crucial.
- To obtain adequate commercial drive circuits for the SiC power switch showed to be much more difficult than anticipated based on available commercial information.

The project generated the following documents and dissertations:

- A PhD thesis to be defended in early 2013
- 1 final project report
- 4 journal articles
- 13 international articles and posters
- 4 international and national popular scientific presentations
- 2 workshops were organized
- 37 part reports and technical notes
- An online database compiling information and datasheets for relevant materials and components were established

The project was started in January 2009 and closed in January 2013. The budget frame for the project was kNOK 8000; kNOK 6400 from the Research Council of Norway and the remaining kNOK 1600 from the project partners. The cost was distributed as shown in Table 1.

Table 1. Projects costs (2012 are budget figures).

	2009	2010	2011	2012	Sum
Personnel and indirect	1180	840	1550	1186	4300
Purchase of R&D services, incl. PhD	23	580	802	800	2500
Equipment	182	240	22	200	800
Other expenses	105	100	80	100	400
Total sum	**1490**	**1760**	**2464**	**2286**	**8000**

The participating members of the project were:

Badger Explorer, Roxar Flow Measurement (Emerson), TranSiC (Fairchild semiconductor), SmartMotor, Techni, Vestfold University College and SINTEF (coordinator, project manager and main scientific contributor).

2 Introduction

High temperature environments offer great challenges for electronic systems. Although the number of commercially available high temperature components, such as wide band gap semiconductors (e.g. silicon carbide) is rapidly increasing, lack of qualified high temperature packaging technologies limits the growth. In other words: To be able to design and build the next generation high temperature electronic systems, incorporating emerging high temperature components such as silicon carbide, novel packaging methods must be developed.

Silicon carbide (SiC) is a well known material that has long been utilized for its hardness (almost as hard as diamond). This material has only recently has been exploited, in its pure crystalline form, for its semi-conducting properties which e.g. enables low loss high power switching. It is also a stable material at high temperatures which make it ideal for high temperature applications or applications with high power densities. SiC is especially well suited for motor control devices inside hot petroleum wells, where both high energy density (dissipated power) and high ambient temperatures are present.

Motor control systems based on SiC technology provides the means to achieve very high efficiency for electrical motor controllers, which reduce power consumption. But, the main advantage given by SiC technology is the possibility for small low weight solutions. E.g. the automotive industry is adapting SiC technology into emerging electric cars.

To be able to build the next generation of high temperature (>200 °C) compatible power switches with SiC components, other components must be available too. Compatible substrates, capacitors, resistors etc., needs to be identified and specified. All these components must also be prepared for the necessary packaging technologies. I.e. it is crucial that the components have the correct metallization scheme, have a proper surface finish, a suitable thermal expansion coefficient etc.

Perhaps the main challenges to build such a system is the need for novel packaging techniques that is stable and robust at high temperatures. The techniques must produce reliable electrical and thermo-mechanical connections to be useful. This is the main theme of the High Temperature Power Electronics Packaging (HTPEP) project.

Traditionally, oil and gas well drilling has been performed by large oil rigs. With powerful motors that may operate downhole, electronically controlled locally, one may envisage simplified and safer drill operations in the future. SiC technology and adherent novel high temperature packaging technologies will enable this vision.

One of the HTPEP project partners, Badger Explorer ASA, develops a method to drill exploration wells without an open hole to the surface of the seabed. The method requests effective electric motors for the drill. They must be controlled locally by electronics to adapt continuously to the changing environmental conditions during drilling. This novel method for well exploration will both improve safety and reduce the environmental risk. But, it has been characterized as a pioneering technology because will drastically reduce cost framework for future well exploration operations. In addition, the energy consumption for operations will be reduced to about one hundreds of today's level.

Oil and gas technology is essential for the Norwegian society, contributing to more than 50 % of the Norwegian export income and 30 % of the public revenue. The Norwegian petroleum revenue secures the welfare for both todays and coming generations. The development of more efficient oil and gas extraction technologies is therefore important for the Norwegian welfare. Knowledge and technology obtained in this area can also be used in other high temperature applications, such as automotive or aerospace.

The field of high temperature electronics is a broad field, covering many disciplines and markets. Thus, there exist numerous applications for high temperature electronics. By increased monitoring and control of engines used in e.g. automobile and aircraft an optimized combustion and reduced fuel consumption may be achieved. The operation temperature of this electronics is in the range from 300 °C to 600 °C. Extended use of electronics during oil and gas exploration will increase the recovery factor and simultaneously decrease

the risk of emissions to the environment. Downhole electronics can experience temperatures up to 275 °C, often in combination with high pressure, vibrations, shock and chemically aggressive ambient media. Other applications for high temperature electronics include space exploration (up to 500 °C), geothermal wells (~ 200-400 °C) and nuclear reactors (~ 200-450 °C).

The main objective for the HTPEP project was investigation and development of packaging technologies for high temperature power electronics. The effort was concentrated around an imagined case for a high temperature power module based on SiC technology.

In general, the project found that packaging technologies for operation temperatures beyond 200 °C are emerging. The main results from the project include development of a state-of-the-art die attach technology, joining a SiC device onto a ceramic circuit board. It was tested up to 250 °C and beyond with convincing results. HTPEP was also showed that efficient thermal designs may be developed that will enable higher operation temperatures and/ or longer life times of the electronic systems in the future.

One of the main conclusions drawn from the project was that electronic components for high temperature operation (200 to 250 °C) are still very sparse. Especially as bare die components they seldom have the option of for state-of-the-art high temperature packaging metallization schemes (typically Au based). The large worldwide effort and interest in high temperature electronics that has developed during the project period will certainly assure that the field of high temperature electronics and packaging will advance at a high pace in the time to come.

Key personnel

The active key members working in the project is presented in Table 2.

Table 2. Key personnel

Name	Title	Role	Period
Andreas Larsson	Senior scientist	Project manager (2010-2012) Project participant (2009)	Jan 2009 – Jan 2013
Torleif A. Tollefsen	Research fellow (PhD)	Task manager – Die attach	Feb 2010 – Jan 2013 PhD ends early 2013
Olav Storstrøm	Research scientist	Task manager – Electronics	Jun 2010 – Oct 2012
Rolf Johannessen	Research scientist	Project manager	Jan 2009 – Jan 2010
Frøydis Oldervoll	Senior Scientist	Project participant (2009) Task manager – Interconnects (Front side) (2011)	Jan 2009 – May 2009 and Dec 2010 – Dec 2011
Astrid-Sofie Vardøy	Master of science	Project participant	Jun 2011 – Jan 2012
Per Schjølberg-Henriksen	Senior Scientist	Project manager	Jan 2010 – Feb 2010

3 Substrate technology

The substrate is the backbone in electronic systems. It provides the electrical isolation and structural support required to build electronic circuits. And as for all packing components, the mechanical strength and long term robustness is essential for a reliable electronic system. Thus, the requirements for the material properties; mechanical, electrical, thermal etc. are very stringent for any high reliability system.

Hybrid substrate technology is a well proven technology that has been employed for high reliability applications for several decades. It has shown great potential up to 200 °C and beyond. It combines a ceramic core (the board) as the isolation layer with a metal layer on the surface (the conductors); traditionally with thick and thin film technologies and low and high temperature co-fired ceramics (LTCC and HTCC). Several approaches have been explored to improve the performance, especially for improved thermal cycling capability, of the ceramic/metal technology including; direct bonded metal, typically Cu or Al (DBC and DBA) as the most common high reliability technologies today. Still, mechanical failures occur frequently when exposed to elevated temperatures for longer time periods. Typical failures are delamination of traces from the surface (adhesive failure) and cracking of the ceramics itself (cohesive failure). This is primarily due to great stress induced in the system by a large mismatch in coefficient of thermal expansion (CTE) between materials. Typically, the CTE for metals are in the region 15–30 ppm/K and for ceramics it is around 3–10ppm/K. Locally, the mismatch can get even more severe by discrete components assembled on the substrate (SiC and Si with a CTE in the region 2–4.5 ppm/K).

In recent years a novel technology, active metal brazed (AMB) ceramics, has appeared with promising adhesive and cohesive properties based on a strong ceramic core. The most common material for the traces are noble metals; Au, Ag and Cu. The core is typically made of silicon nitride or aluminium nitride. This technology is promising and feasible for future high temperature applications.

Another interesting technology worth mentioning is μ-DBC that emerged during the project. It is similar to the standard DBC technology, but the metallization thickness is thinner, < 50 μm, than for normal DBC. This makes it more compliant to thermo-mechanical loads, i.e. generates lower stress, than standard DBC substrates. It has shown promising high temperature cycling results compared to DBC [De Langlade ATW 2011]. Compared to AMB substrates it might offer improved design rules, e.g. allowing a finer pitch. Since, the chosen substrate, silicon nitride AMB, showed excellent results throughout the project, μ-DCB was never investigated further but might be explored in future projects.

3.1 Materials and methods

3.1.1 Silicon nitride active metal brazed, Si_3N_4 AMB

The substrate technology chosen for the HTPEP project was a silicon nitride, Si_3N_4, with active metal brazed conductors.

Si_3N_4 is low to medium cost ceramic substrate material commonly used when high mechanical strength (~900 MPa in flexural strength) combined with high thermal conductivity (90 W/mK at room temperature) is requested. It has a matching CTE; ~3.5 ppm/K, to SiC, Si and ceramic components. The substrate has shown great thermal cycling capability surpassing all other competing technologies, Al DBC, Si_3N_4 DBC, Alumina LTCC etc. The high thermal conductivity combined with substrates as thin as 300 μm provides excellent thermal properties with a low effective thermal resistance; typically in the magnitude order of 10 mm^2K/W. The substrate may be produced with both Au and Cu conductors, but the Cu alternative is more readily available.

The active metal braze technology may be described by that a sheet of metal is brazed with a solder onto the ceramic core at a process temperature around 600-800 °C creating strong adhesion between the metal and ceramic. The substrate is typically thermally balanced with a symmetric pattern on the back side to minimize warpage and reduce residual stress from the fabrication process. Due to the design rules, this back side

pattern may not always be a perfectly symmetric design, i.e. including mirrored traces. Denka was one of the first suppliers of Si_3N_4 AMB substrates and holds several patents on the technology. Competing companies, Kyocera and Rogers (curamik), has developed their own technology offering similar products as Denka (they are also referred to as AMB ceramics). In addition to the Denka substrate, they now offer other interesting and attractive options as well, such as finer pitch and multi layer structures. This could be interesting for future applications.

3.1.2 Substrate and metallization scheme

The investigated substrate was delivered by Denka chemical. Kyocera was also contacted to supply substrates for evaluation, but we were unable to attain any samples. The metallization for the substrate was based on a traditional ENIG process (Ni plating with immersion Au) on the Cu surface. Additional thickness of the top Au layer was added to prepare for the Au-Sn SLID process, described further in section 4.

Dummy substrate – The investigated substrate metallization system is shown in Figure 1. The layer functionality is presented in Table 3.

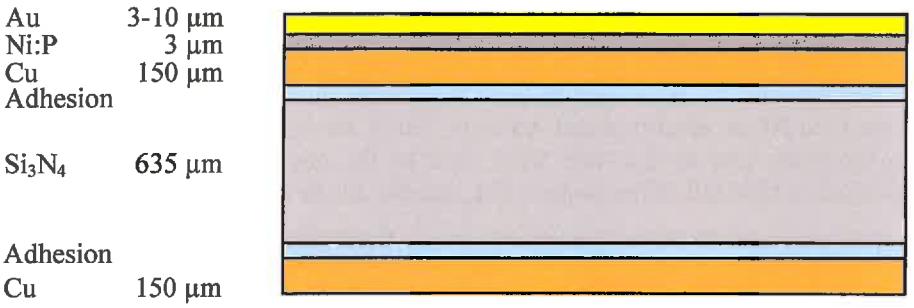


Figure 1. Substrate metallization scheme.

Table 3. Functionality of the individual layers in the substrate stack in Figure 1.

Layer	Functionality	Comment
Au	Bondable surface Compliant (mechanical absorption) Diffusion barrier between Au and Sn Anti-oxidation	This is further explained in section 4.
Ni:P	Diffusion barrier between Cu and Au	7wt%P
Cu	Circuit layer Thermal balance	Front side (top) Back side (bottom)
Adhesion	Adhesion to ceramic	Propriety material. Patent [US 2009/0283307 A1] states that Ag and Cu and an active metal are used. Active metals include; Ti, Zr, Hf, Nb, Ta, V and compounds thereof.
Si_3N_4	Structural Electrical isolation	

Final substrate – The final circuit board (Figure 2), designed for the case study, had the same structure as the dummy substrate but was ordered without the Ni layer because it was not possible to get Ni only on the front side of the substrate. The possibility for a Cu / thermal interface material (TIM) / Cu joint between the

substrate and base plate requested the back side surface was to have bare Cu. This option was attractive for two reasons; first the chosen TIM would only have been compatible with one surface material and secondly there exists several adhesives suitable to bond to Cu.

Electro-plating was planned to build the required Ni and Au layers. The electro-plating process was unfortunately never attempted since we never found a practical way to manage this. Several methods were tried.

Au wire bonds to the Cu surface were tried to electrically connect the isolated traces on the surface to prepare the substrate for electro-plating. It gave too low yield with unreliable bonds.

Ti has shown to be a suitable diffusion barrier between Au and Cu for HT applications. Thus it is feasible to replace the Ni with a Ti layer. At least 100 nm Ti is required for the barrier. 200 nm Ti and 200 nm Au was applied with chemical vapour deposition (CVD) on the Cu surface. CVD does not require electrical connection between the traces. A simple peel test using regular office Scotch tape was used for a first inspection. The results were unsatisfactory with poor adhesion of the Ti to the Cu surface. This may either come from possible residual stress or perhaps from adhesive residues from the masking tape (Kapton). Ti is known from the Si industry to easily create high residual stress in the interface unless the process is optimized.

An attempt to deposit 1 µm Ni followed by 200 nm Au by chemical vapour deposition (CVD) was initiated. The traces covered with the 200 nm Au layer should have been interconnected with Au wire bonds to prepare the subseries for the final 10 µm electro-plated Au layer. Au to Au wire bonds is a standard process which should not be any problem. Due to the high work load of the operator of the CVD equipment combined with the short amount of time left of the project, this process was never investigated.

Another alternative was also proposed to solve the plating issue. Cambridge University in the UK was contacted, since they have equipment and experience to deposit similar metals, and they were positive to have a go at it, but unfortunately there was neither time nor resources to follow this path before the project end.

Alternative approaches, such as, custom made structures with spring loaded pins to create electrical interconnection between the traces to prepare the samples for electro-plating were suggested but never realized.

Chemical plating was another option, but it is uncertain if the required thickness of the layers is feasible to build by this method.

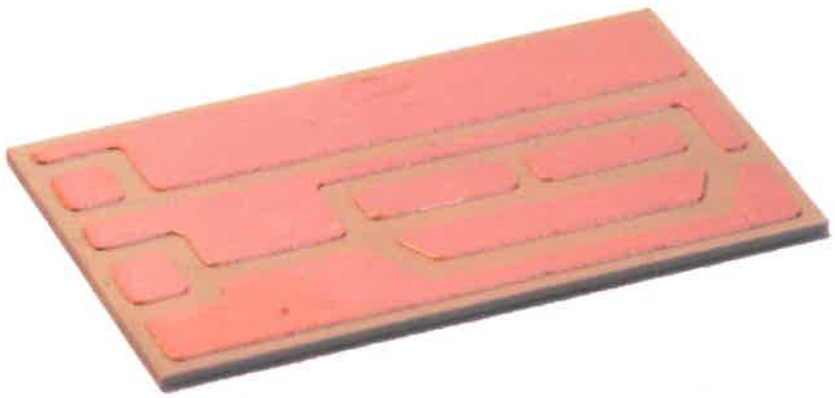


Figure 2. Fabricated substrate for the case study. Without the Ni / Au top layers.

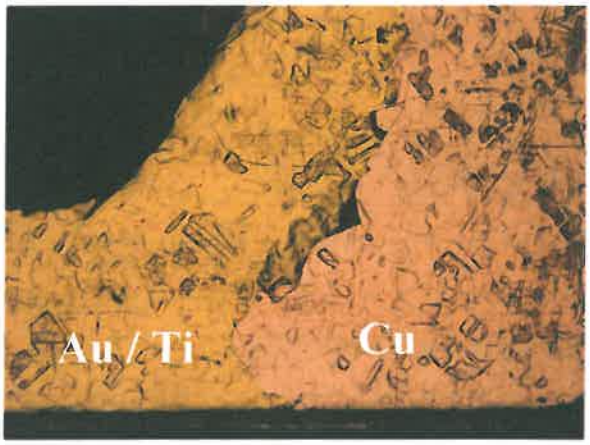


Figure 3. Micrograph of the surface of the final substrate with CVD deposited Ti and Au after a peel test. The exposed Cu surface beneath the Au /Ti layer is clearly visible.

3.2 Results and discussion

Simulations

The final substrate design of the circuit board for the case study was investigated by finite element analysis performed in COMSOL Multiphysics. The substrate was assumed to have a strain reference temperature at room temperature (RT). An initial analysis, A, showed potential warpage of the substrate when exposed to operation temperature, $T_{operation}$ (Figure 4). The thermo-mechanical stress inside the substrate was also analysed for a possible case, B, when the substrate was exposed to a bond process temperature, $T_{process}$, of 300 °C, securing the substrate to a AlSiC base plated with a Cu-Sn SLID bond and then taken back to room temperature, T_{RT}. A third case, C, investigated the thermo-mechanical stress during operation, $T_{operation}$, at 220 °C for the same Si_3N_4 / Cu-Sn / AlSiC system. The analysis showed that the substrate was tending to bend and warp due to the mismatch in coefficient of thermal expansion (CTE) within the system. I.e. the additional stress inside the joints from the warpage in a final system may reduce the system life time or in worst case cause catastrophic mechanical failure in the interconnects. The warpage also resulted in high plastic strain, ~ 20 %, inside the Cu layers (Figure 5). This is in the region of to the maximum elongation at break for Cu; 10-50 % depending on process and material quality. This indicates that there might be a cohesive fracture at the corners of the Cu traces on the substrate. Adhesive failure inside the adhesion layer between the Cu traces and ceramic core also seems possible. Additional information of the analysis of case B and C may be found in [Larsson HiTEC 2012] and in section 6.

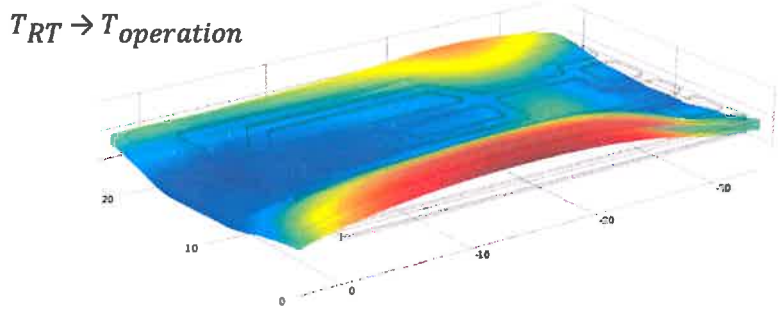


Figure 4. Potential warpage at operation temperature assuming strain reference temperature at room temperature (RT) for case A. The deformation in the figure is amplified by a factor of 100. The maximum peak-to-peak deformation was up to 40 µm.

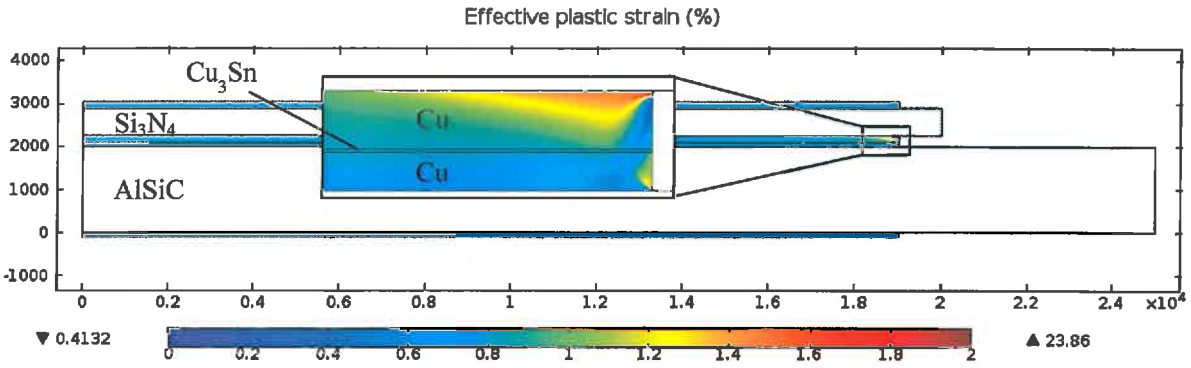


Figure 5. Effective plastic strain inside the metal layers at room temperature after a Cu-Sn SLID bond process (case B). The effective plastic deformation may reach up to ~20 %.

Experiments

Dummy substrate – The die attach, metallization scheme and substrate are closely coupled in realistic applications. Therefore, the substrate was mainly investigated by experiments in the configuration shown in Figure 8. The stack was exposed to 1000 thermal cycles between 0 to 200 °C, stored at 250 °C for up to 6 month and stored at 250 °C for 3 month followed by 1000 thermal cycles between 0 to 200 °C. Not a single substrate of the more than 100 tested samples that were exposed to the thermal aging tests showed any sign of degradation or failure.

Final substrate – The final substrate (without Ni and Au) was attached with an adhesive to an AlSiC base plate and stored at 250 °C for 2700 hours without any signs of delamination or cracking or any other failures. More information about this experiment is found in section 7.

The simulations suggested that there might be cracks at the corners. No such cracks were found for the real substrates exposed to 250 °C for 2700 hours. A visual inspection by optical microscopy for these cracks was performed.

4 Back side interconnect (die attach technology)

The choice of interconnect technology, i.e. the conductive path required to achieve connection from a circuit element to the rest of the circuit, is of utmost importance in electronic devices. Commonly used interconnect techniques include solders, welding and conductive adhesives. However, for high temperature (HT) applications, the standard interconnect materials do not meet the requirements regarding e.g. high temperature stability. There is a limited range of high temperature interconnect techniques. One alternative is sintered nano-particle Ag, which has good electrical and thermal conductivity. A nano-particle Ag joint has a high melting point (960 °C) compared to the low processing temperature (< 300 °C). However, Ag migration is reported to be a problem in high temperature applications (particularly in combination with high power) combined with a non uniform joint with pores, limiting the lifetime of the joint. Another interconnect, solder type, that has shown interesting high temperature results is eutechtic Au-Ge which melts at 361 °C and therefore is a potential high temperature candidate for operation above 200 °C.

Other prospective high temperature interconnect techniques include liquid-based solder joints, composite solder joints, bismuth-based solder joints, and solid-liquid interdiffusion (SLID) joints. Of these techniques, SLID bonding – also called Transient Liquid Phase (TLP) bonding, isothermal solidification, or off-eutectic bonding – has shown great potential. The SLID technique uses a binary system consisting of two metals with different melting points T_{low} and T_{high}, and relies on the formation of intermetallic compounds (IMC). At a processing temperature above T_{low}, IMCs will form. They will have a higher melting point than T_{low}, giving bonds that are stable above the processing temperature. The general principles of the SLID bonding process are illustrated in Figure 6.

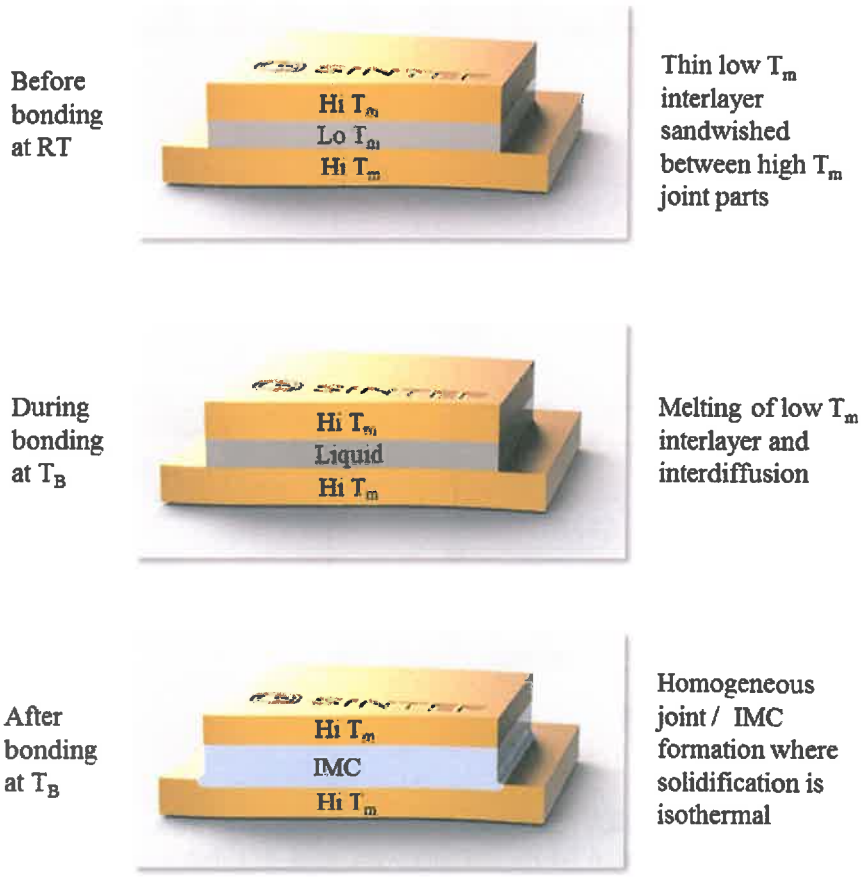


Figure 6. Schematic illustration of solid-liquid interdiffusion (SLID) bonding (T_B: Bonding temperature, T_m: Melting temperature, RT: Room temperature, IMC: Intermetallic compound).

4.1 Au-Sn bonding

SLID bonding has been performed in various metal systems. Examples include Ag-In, Ag-Sn, Au-In, Au-Sn, Cu-Sn and Ni-Sn. Ag-In, which is among the first SLID systems, has been investigated for high temperature applications in several studies. Here, a high temperature stable joint can be achieved (stable up to 700 °C) using a processing temperature of only 210 °C, followed by annealing at 150 °C . However, the high temperature lifetime of the joint is reported to be limited (especially in combination with high power), due to Ag migration.

Au-Sn is a promising SLID system for high temperature applications. Based on the Au-Sn phase diagram (shown in Figure 7), several Au-Sn phases can be appropriate for high temperature applications. However, when long time stability is taken into account, the ζ phase is the most promising. The final bond structure was reported to be layered – Au / ζ' / Au – where the ζ' phase undergoes a phase transition to the ζ phase at 190 °C. The ζ phase has a melting point of 522 °C, making it desirable for high temperature applications. Thorough investigations of the Au-Sn phase diagram suggests that the actual layered bond structure probably is Au / ζ / Au, since the ζ phase is stable down to -5° C (depending on Au concentration). Another possible bond structure is Au / β / Au. The β phase has an even higher melting point than the ζ phase, i.e. 532 °C. However, the ζ phase is reported to be tougher (more fracture resistant) than the β phase, indicating that a Au / ζ / Au bond probably is more reliable than a Au / β / Au bond. Au-Sn SLID has already shown good high temperature stability and thermal cycling abilities in studies performed by Johnson *et al.*

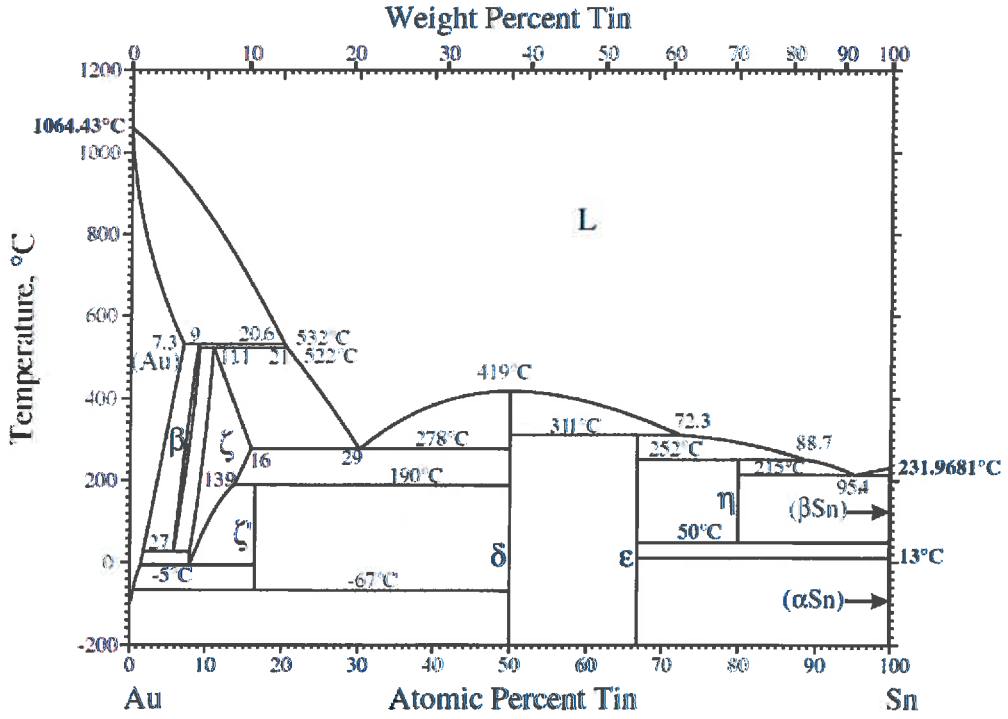


Figure 7. The Au-Sn phase diagram.

4.1.1 Materials and methods

The material stack for the die / die attach / substrate is shown in Figure 8. Si_3N_4 substrates with active metal bonded (AMB) Cu (150 µm) and plated Ni-P (7wt%P) were used as substrates for all SLID samples. The substrates had symmetrical metallization (Cu / Ni-P layers on both top and back side) to minimize warpage of the substrate due to coefficient of thermal expansion (CTE) mismatches between Si_3N_4 and Cu. An additional Au layer (3 to 10 µm) was electroplated on the substrates in a gold cyanide solution at a

temperature range of 60-65 °C, with a current density of 2.7 mA/cm^2. The substrate was diced in 6x6 mm^2 samples after plating.

The BJT SiC dummy chips, delivered from Fairchild, had a sputtered Ni_2Si / Ni / Au metallization (cf. Figure 8). The chips were electroplated with a uniform Au layer (5 to 10 µm), and diced in 1.855 x 3.4 mm^2 samples.

Assembly was performed in two steps; first, the substrate, the eutectic Au-Sn preform (80:20 wt%) and the chip were aligned manually on a hot plate and fastened with a clamping force corresponding to 2.5 MPa on the surfaces to be bonded. Secondly, the samples were bonded using a hotplate. Bonding was performed in a vacuum chamber (chamber pressure 10 kPa / 75 torr). The samples were heated to 250 °C and held there for 5 min (to bake out any residual moisture and to assure a uniform temperature distribution in the bonding layers). Then, the samples were heated to 350 °C, and kept there for 5-20 min to ensure that the desired phases were created

Die shear testing is a technique to determine the integrity of materials and methods used to attach semiconductor die or surface mounted passive elements to substrates. It is among the most commonly utilized bond strength characterization methods. The method is effective regarding cost and time.

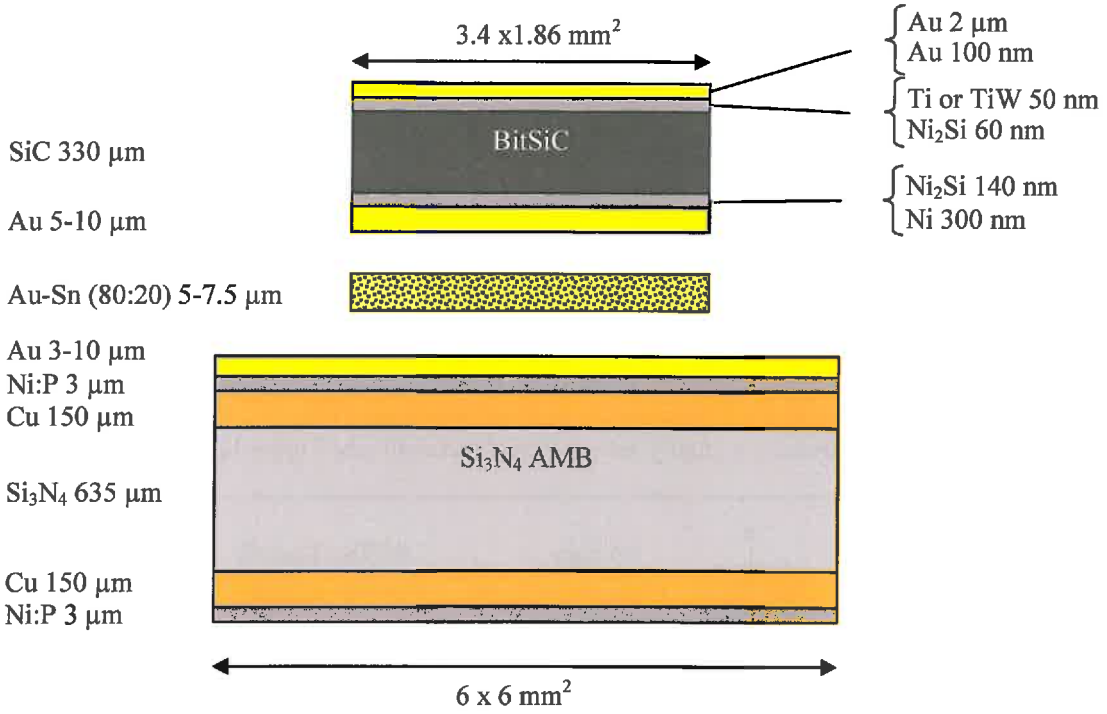


Figure 8. Investigated stack with a dummy SiC component on the top attached to the Si_3N_4 AMB substrate with the Au-Sn SLID bond.

The subjected samples were exposed for different environmental tests to investigate their reliability. High temperature storage (HTS), a test to examine the reliability of the subjected packages at specified conditions over an extended time period, was performed at 250 °C in air for 1, 3, and 6 months. This test is very important for high temperature packages, since high temperature environments will accelerate intermetallic diffusion and creep mechanisms. This can result in the formation of new brittle intermetallic compounds (IMCs), Kirkendall voids (the formation of voids due to a difference in diffusion rates), or void and/or crack formation generated from creep, which all will reduce the reliability of the subjected package.

Thermal cycling (TC), a test to determine the resistance of the package at extremes of high and low temperatures, and the effect of alternate exposures to these extremes, was performed. The test exposes the package to mechanical fatigue induced by coefficient of thermal expansion (CTE) mismatches in the package. Important parameters besides the temperature extremes include the dwell time and the transfer time between temperature extremes. It is important that both the dwell and transfer time is long enough to ensure approximate structural equilibrium in the materials in the subjected package. Thermal cycling was performed on selected samples between 0 – 200 °C, with a gradient of 10 °C/min, and a dwell time of 15 min at the temperature extremes.

A combination of HTS and TC was also performed. If a package is intended for an application experiencing both high temperature and temperature variations, it will be important to test the same samples for both storage and cycling. Storage can induce a phase transformation in the die attach and interconnection materials. It is therefore important to verify that stored samples also can withstand the mechanical fatigue introduced during thermal cycling afterwards.

4.1.2 Results and discussion

It has been demonstrated that Au-Sn SLID bonding is an excellent die attach and interconnect technology for high temperature applications. It has also been shown that Au-Sn SLID can withstand large temperature variations in a packaging system with large residual thermo-mechanical stress (induced by CTE mismatches). Other technical contributions include:

- Demonstrated high shear strength, about 70 MPa, after high temperature exposure at 250 °C and after cycling between 0-200 °C (see Figure 9).
- Demonstration of the importance of a symmetric Au-Sn SLID bond, and excess Au (compliant layer) on both chip and substrate (see Figure 9).
- Optimization of bonding parameters (temperature 300 °C, total bonding time (above eutectic melting point) 6 min), and demonstration of the importance of conducting the bonding in absence of O_2.
- Optimization of the geometry / thickness of the Au and Au-Sn layers in a SiC / Ni / Au / Au-Sn / Au / Ni / Cu / Si_3N_4 package regarding thermo-mechanically stresses induced by CTE mismatches.
- Shown how the bond configuration of a Au-Sn SLID bond changes at different stages during high temperature exposure, from the ζ-phase to the β-phase (see Figure 11).
- Shown that the shear strength is greatly temperature dependent (see Figure 12).

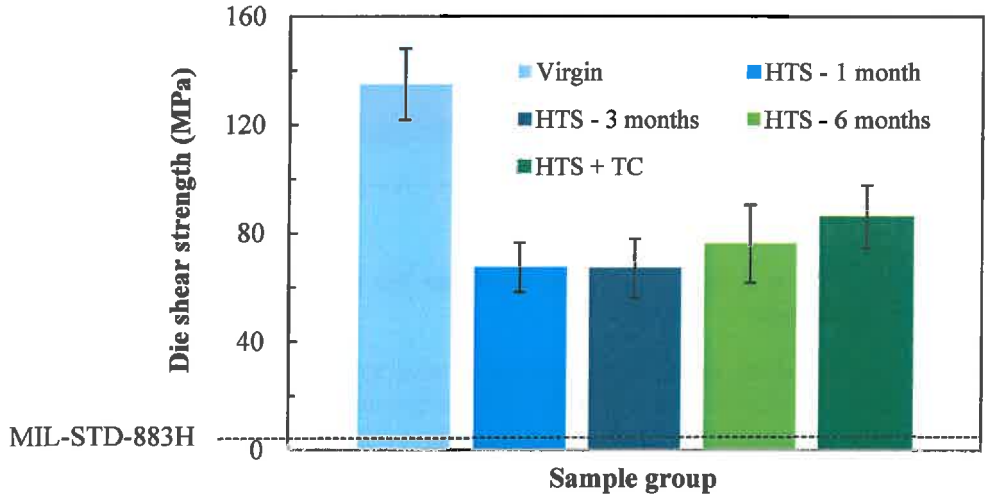


Figure 9. The shear strength of the optimized Au-Sn SLID samples (Virgin) after and thermal ageing (1, 3 and 6 months at 250 °C) and a combination of thermal aging (HTS) and cycling thermal cycles (TC) (0 – 200 °C, 10 °C/min, dwell time of 15 min).

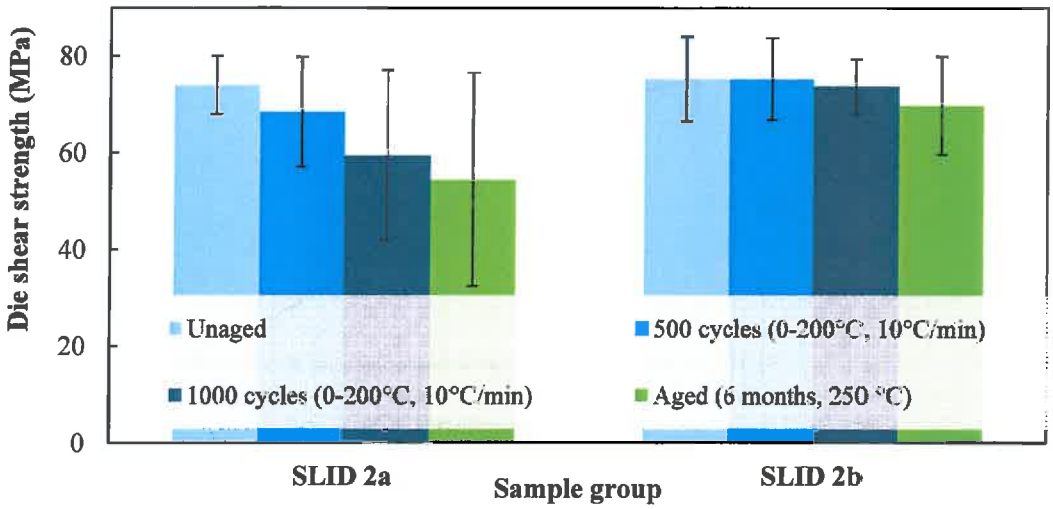


Figure 10. The shear strength of Au-Sn SLID samples as a function of the number of thermal cycles (0 – 200 °C, 10 °C/min, dwell time of 15 min) and thermal ageing (6 months at 250 °C). Note that this figure is only included to visualize the main trends. Since many of the tested samples did not fracture during testing, due to the equipment limit (50 kgF), a proper average cannot be made.

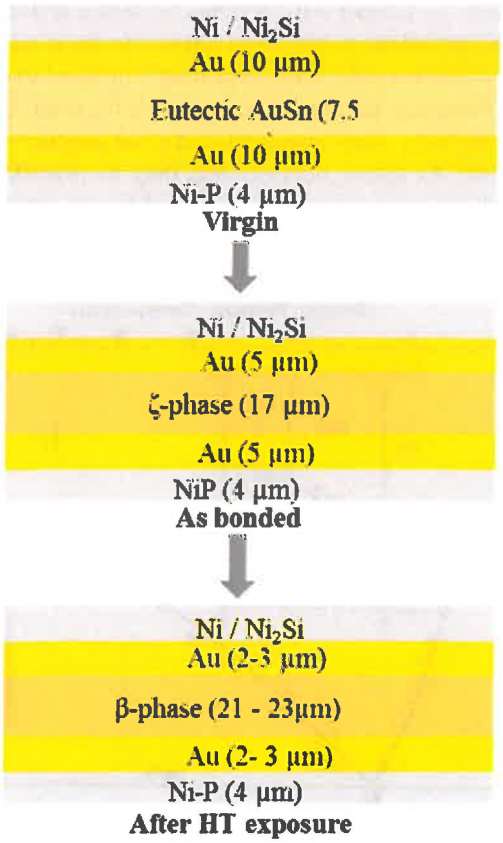


Figure 11. A schematic overview of the layered structure of an optimized Au-Sn SLID bond at different life stages. The different material phases were identified with energy dispersive spectroscopy (EDS) and x-ray diffraction (XRD).

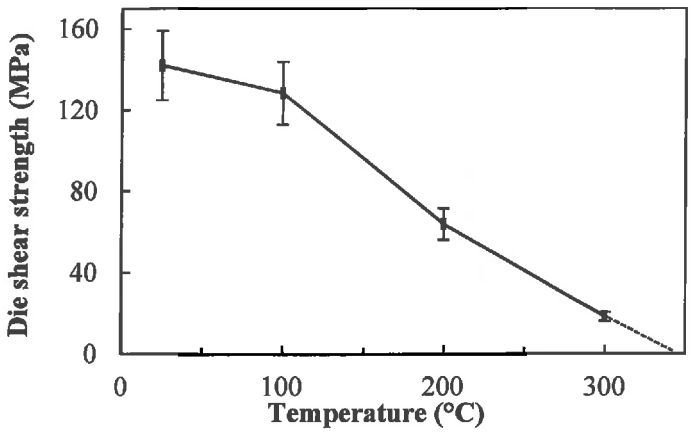


Figure 12. The average shear strength of Au-Sn SLID samples as a function of temperature. Each point is based on six measured samples. The dotted line represents an extrapolation of the line to indicate the effective melting point of the bond.

4.2 Au-Ge bonding

Eutectic Au-Ge (88:12 wt%) has an eutectic melting point at 361 °C which makes it possible to use for high temperature applications above 200 °C. Unlike Au-Sn it has no stable phases to higher temperatures than the eutectic point (see Figure 13). Nonetheless it has been shown to be a reliable die attach material at high temperatures. Banu *et al.* showed that it could withstand tough thermal cycling (4000 cycles between -170 °C to 270 °C with 40 °C/min) without any failures as a die attach for a SiC Schottky diode (of similar size as the dummy BJT chip) to a BeO substrate. They also qualified it for junction temperatures above 300 °C. This makes it a suitable high temperature die attach material that may be reworked and used on components with thin Au layers (less than a couple of µm) where Au-Sn solid-liquid interdiffusion (SLID) will not work. Unfortunately, thick Au layers (> 1 µm) on components are sparse today. This may limit the potential use of the SLID technology.

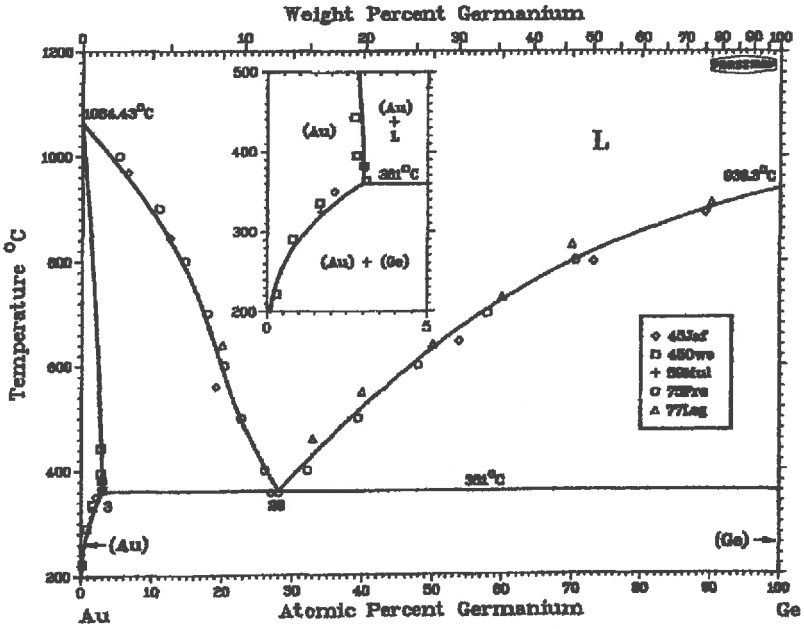


Figure 13. The Au-Ge phase diagram.

4.2.1 Materials and methods

The same test system was used as for the Au-Ge bond as for the Au-Sn SLID bond, only with a 25 μm thick and 1 mm wide eutectic Au-Ge foil instead of the Au-Sn preform (cf. Figure 8). The bonding was performed on a desktop hotplate in a regular lab (Figure 14). It was performed in a N_2 atmosphere to avoid O_2 contaminating of the surfaces, prior and during bonding. The bonding was performed at process temperatures at around 450 °C. The bond process was never optimized.

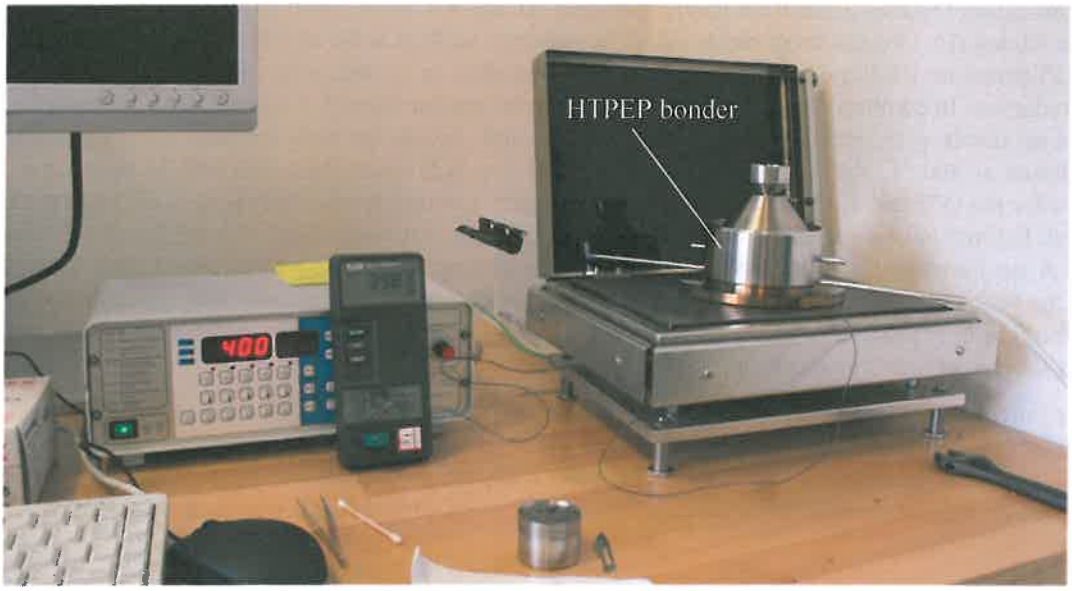


Figure 14. Photograph of the setup during bonding of a Au-Ge test sample (initial bonding in progress).

4.2.2 Results and discussion

The bonds created were as strong as suggested by the literature, around 50-60 MPa, thus the process was believed to be good enough. The typical fracture surface seemed to be in the Ni_2Si layer on the SiC dummy chip which was odd since this was not observed for the Au-Sn SLID samples. Perhaps it was due to the high process temperature? It was hard to tell whether the fracture was adhesive or cohesive. A typical fracture surface is shown in Figure 15.

Figure 15. Micrograph of the fracture surface for a sample bonded with eutectic Au-Ge.

5 Front side interconnect (wire bonding)

The most common wire bond materials are Au and Al. Both Au and Al have shown interesting results for high temperature applications, but the combination of Au and Al creates a weak brittle phase: $AuAl_2$ often called purple plague. One advantage of using Al instead of Au is that larger wire diameters of the Al wire are available compared to Au wires, hundreds of µm compared to tens of µm. This reduces the current density inside the wires for an equivalent current, i.e. inhibiting electromigration. But combining Al wires with a Au top metallization requires a diffusion barrier between Al and Au. Ni is a well known high temperature barrier between Al and Au. One the other hand, since the substrate surface is Au and the other components also have Au metallization on the terminations/ pads, the monometallic Au system seems far more attractive and much more predictive. In addition, Au suffer less from electromigration than Al. Johnson *et al.* have shown that Au to Au wire bonds may provide reliable and high strength bonds for high temperature applications. After 10000 hours at 300 °C the bonds still managed from 5 g pull force (MIL-STD-883H states that 2.4 g is accepted for the Ø25 µm Au wires used by Johnson *et al.*). Limited Au-Au diffusion at the interface has been observed. Estimation showed that a minimum of five Ø50 µm Au wires should be enough for the case study (I_c < 10 A per transistor) to avoid significant local joule heating, keeping the local over-temperature ($\Delta T \approx 30$ °C) of the wires at bay, as well as securing a comfortably low current density (<1 MA/cm^2) to minimize electromigration. (Typically, current densities >1 MA/cm^2 at 300 °C for time periods of month are used to perform accelerated tests on electromigration.)

Another interesting variant of wire bonding are ribbon bonding which is very similar. A foil with a rectangular cross-section is thermo-compression bonded to the surface instead of wires. This provides a way to get large cross-sections of pure Au interconnect system, reducing the current density, i.e. avoiding possible electromigration issues. Au wire bonding is far more common and readily available than Au ribbon bonding.

Worth mentioning also is that Cu wire bonds have been given much attention in recent years, opening for a possible pure Cu system in the future. This system is still under development for normal temperature applications.

5.1 Materials and method

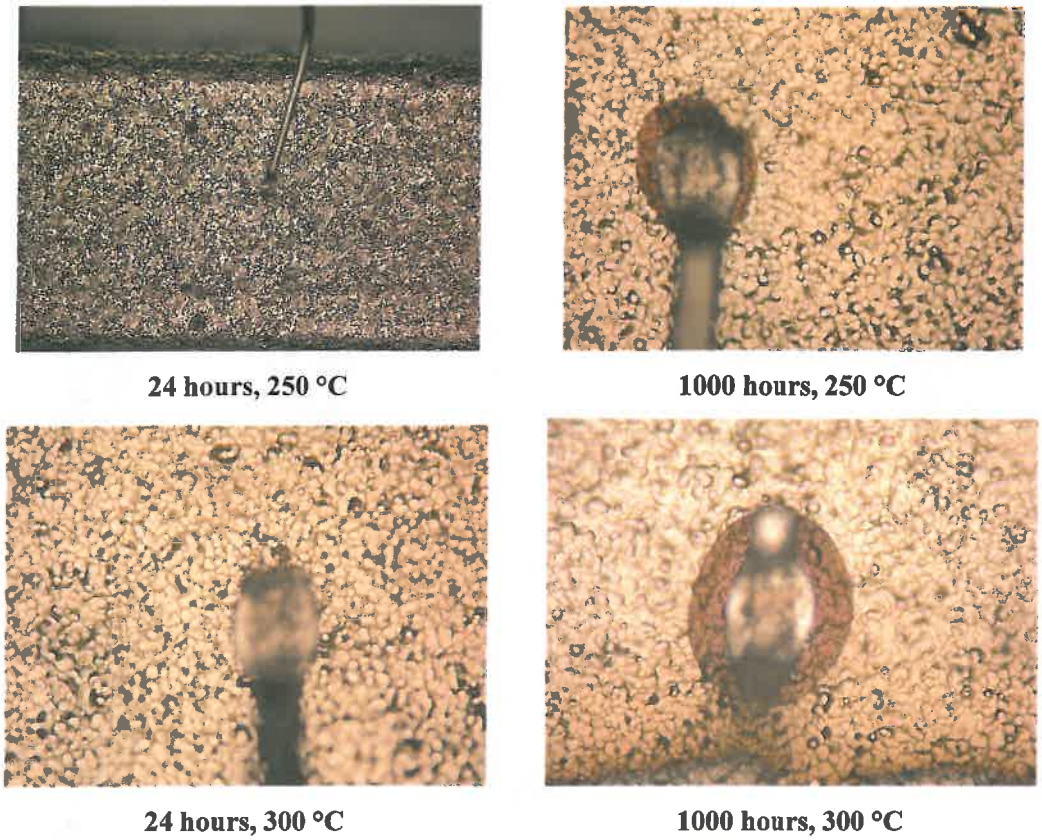
Al metallization are the typical contact metal on common components (most often without Au as an option). It was also believed that Al wire bonds were required for the CISSOD bare die chipset (they had most likely Al as top metallization, cf. section 8). As mentioned in the pervious section, Au wire bonds to Au pads had been investigated with good results for high temperature applications already. Therefore, Al wire bonds were chosen for investigation. The alumina test substrate was alumina with silver thick film (Heraeus C8717B) and cover varnish (Heraeus GPA 200900). The silver metallization was plated with Ni and Au (ENIG process). Process details and layer thickness are not known. This plated thick film system was developed by Norbitech and NJ Innovation and it was interesting to see how an Al wire bond would behave under high temperature conditions. The used substrate was not designed for our test purpose. But, it was possible to use for a pure mechanical test of wire-bond strength before and after high temperature exposure.

Figure 16. Test substrate for wire bond evaluation tests.

Wedge-wedge aluminium wire-bonding with a 25 µm diameter aluminium 1% silicon wire was used for testing. The loop height was 0.4 mm and the loop length was 1.5 mm. The samples were stored at 250 °C and 300 °C for up to 1000 hours.

5.2 Results and discussion

Microscopy – The samples were visually inspected in an optical microscope. In general, a change of colour was observed after thermal ageing, the gold surface was replaced by a darker surface. After 1000 hours of storage a change of colour was observed around the bonding site, a red area appears around the aluminium foot, see Figure 17. After 1000 hours at 300 °C. A colour change along the edges of the plated pads was observed.



24 hours, 250 °C **1000 hours, 250 °C**

24 hours, 300 °C **1000 hours, 300 °C**

Figure 17. Microscopy images of bonding site after high temperature storage (HTS).

Pull testing – 20 bond-loops were pull tested for each ageing condition. The initial pull strength value was lower than expected, with an average value of 4 gram. (Similar systems usually show 8 – 10 gram and MIL-STD-883H require 2 g.) This was derived to originate from that the substrates had been stored for 10 months in office conditions (this should typically not affect the bondability). After high temperature storage the bond strength decreased, the decrease was larger for the samples stored at 300 °C than for the 250 °C samples, see Figure 18. Before ageing and after 24 hours storage the majority of bond failures were in the heel of the first bond. After 1000 hours of ageing 50 to 60 % of the failures were bond lift (i.e. the complete wire-bond is lifted off the surface), see Figure 19.

Cross-section – The bonds were cross-sectioned and inspected by optical microscopy, scanning electron microscopy (SEM) and by energy dispersive X-ray spectroscopy (EDS or EDX). The cross-section revealed a new intermetallic face at the interface between the wire bond and the pad on the substrate. Figure 20 show

a collection of SEM images at the heel. No Au was found in the bond interface but some Au remained just next to the bond interface.

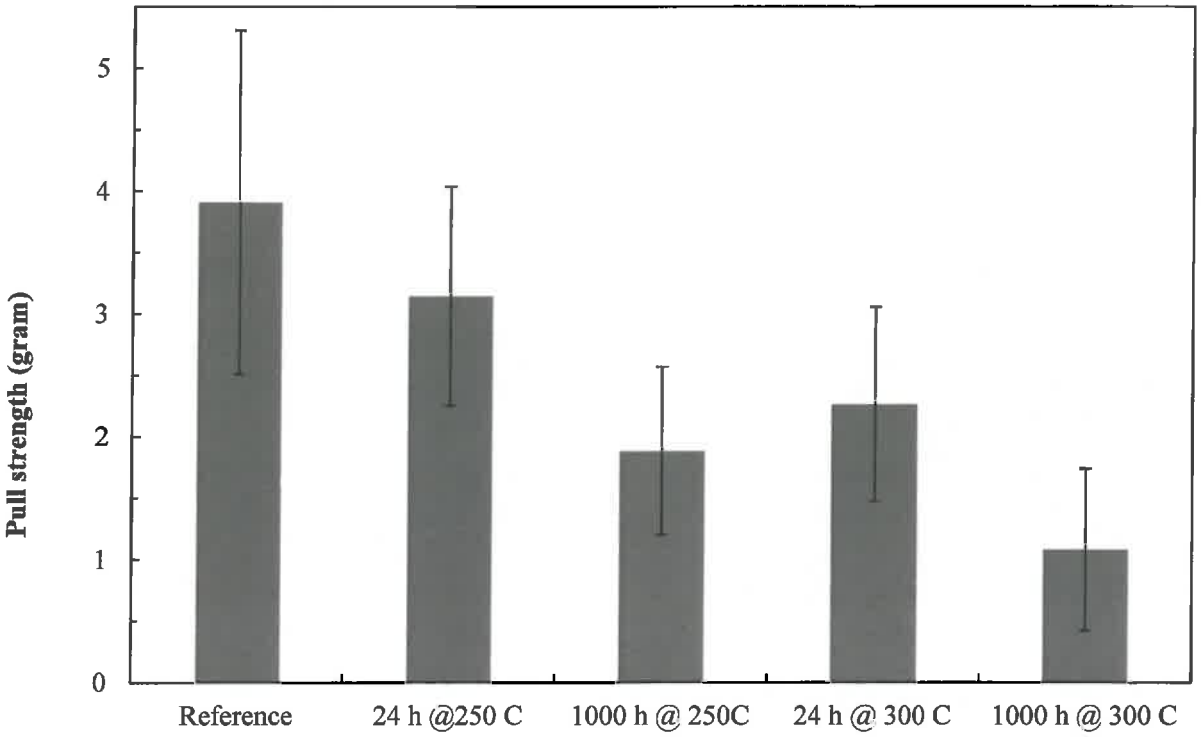


Figure 18. Wire bond pull values.

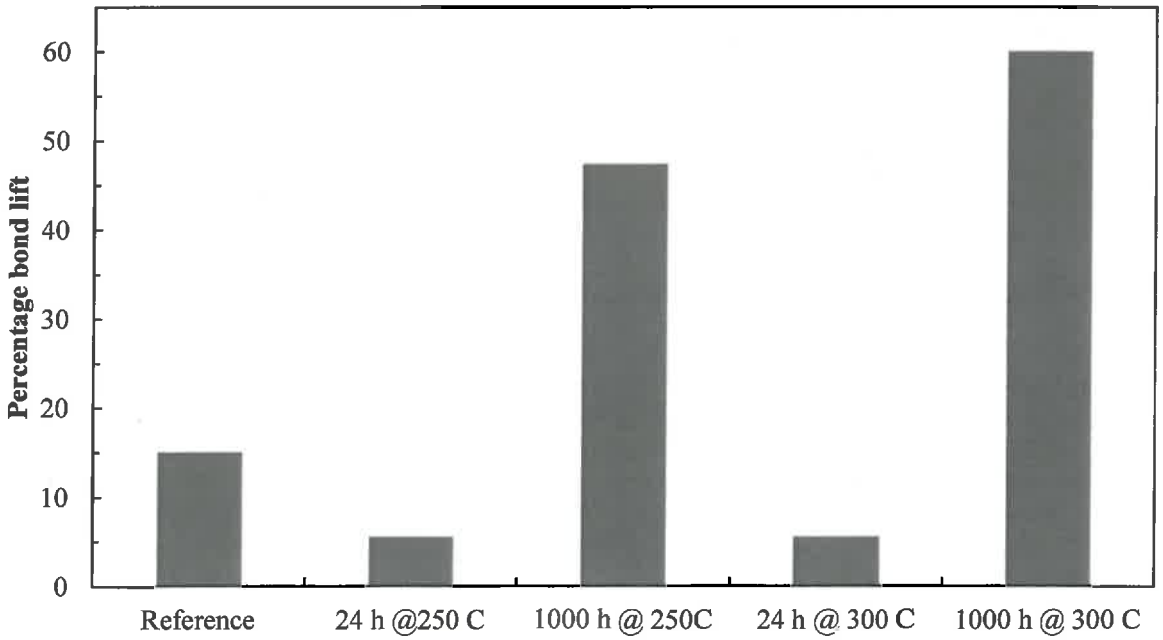


Figure 19. Percentage bond lift.

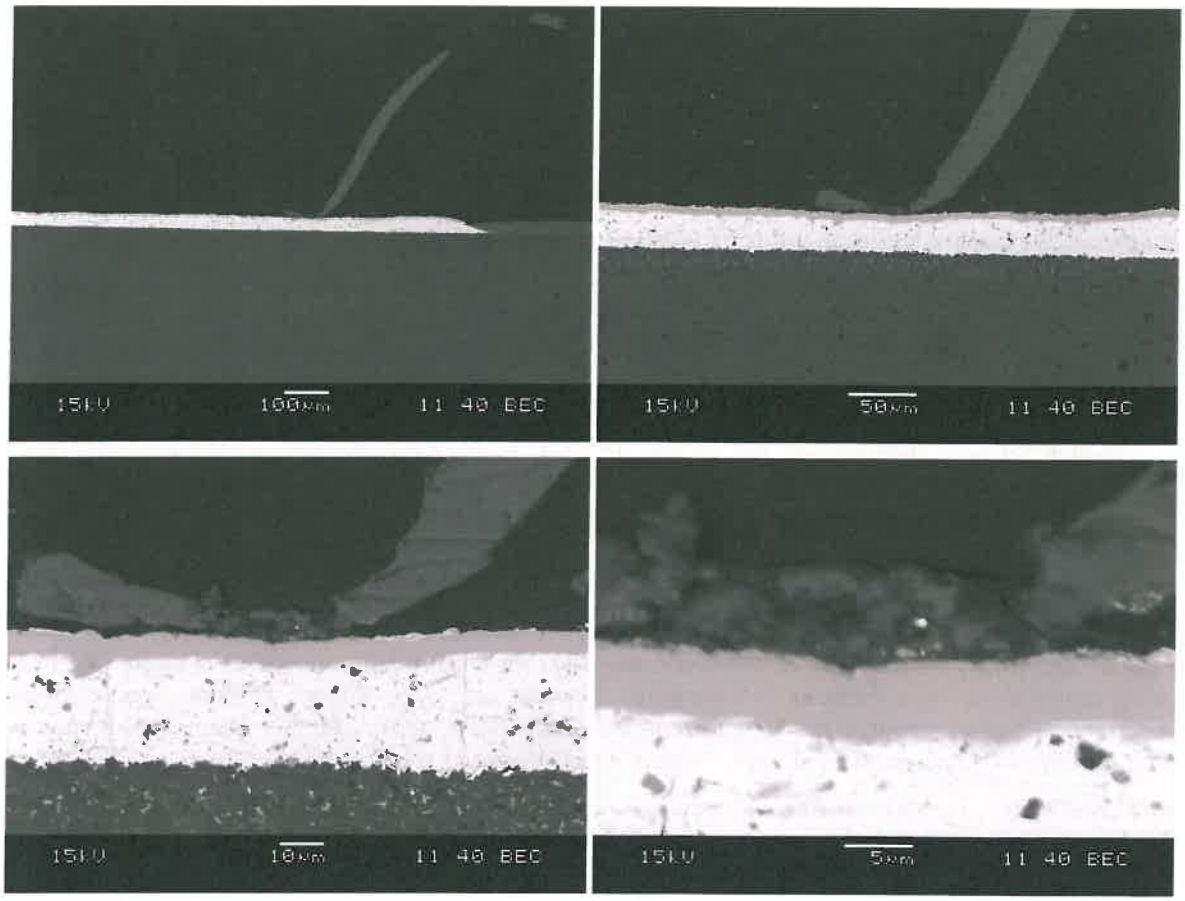


Figure 20. SEM images of the bonding thread and the bonding with the substrate.

6 Encapsulation

Hermetic encapsulation, e.g. by potting materials or forming a solid enclosure with a cavity inside, around the electronic system is a common way to control the environment for the electronics. The cavity may either be evacuated or filled with a compatible material e.g. inert gas, gel or electronic liquid. Such enclosures require structural materials that are compliant with the materials inside the cavity, especially the circuit board. The package materials must also provide sufficient heat transfer capability to avoid high over-temperatures of the electronics inside that encapsulation.

There are several different packaging levels inside a complete package system that needs encapsulation materials. Examples of methods are; conformal coating, molding/ potting and sealants. These materials are typically polymers in various forms. PEEK, PEK and polyimide are common high temperature compatible examples. All polymers have a glass transition point, T_g, at which the material properties may change drastically. E.g. the CTE typically increases from tens of ppm/K to more than 100 ppm/K which cause a severe mismatch between materials and the strength of the polymer typically decrease significantly. Other crucial generic material properties of polymers that must but considered for reliable high temperature operation are decomposition temperature, T_d, and outgassing. Outgassing has proven to be a disingenuous issue that must be tested in in-situ like setups, such as in hermetic chambers together with the active electronic system. (Inside normal open ovens the gasses simply dissolve in the surrounding air and the potential long term effects are not captured.)

There are a vast number of suppliers of polymeric materials for encapsulation purposes. Some of the most interesting suppliers for high temperature compatible materials are; SCS, Victrex, DuPont, Greene Tweed and Lord. They all offer potential products for continuous operation above 200 °C. The materials may be applied in various ways; pored, painted, spray coated, vapor deposited, molded etc.

Structural materials – To build an enclosure around the electronic system materials with an excellent CTE match to an attached circuit board are crucial to design a robust and reliable system. The material must also have a high structural integrity and its porosity shall be very low. There are plenty of common ways and materials to build such structures. One may use the ceramic board itself as a structural component, building walls with a lid on top of it, or one may create a complete enclosure putting the circuit board inside it. Both options have advantages and disadvantages. Common high temperature compatible materials used for this include alumina (Al_2O_3), Kovar and common lead frame materials such as CuMo. AlSiC is a material with attractive thermo-mechanical properties which can be exploited for encapsulation purposes. It is typically used in electronic base plates (often in cold plates). Other novel materials include; nano and diamond composites which have extremely high thermal conductivity (>500 W/mK) combined with low CTE (<10 ppm/K).

Sealant - A high temperature compatible seal is typically soldered or brazed of with a metal solder, e.g. eutectic Au-Sn or Au-Ge, or welded. But polymers are also common, especially for lower temperature ranges. The scale factor of the enclosure requiring a seal sets stringent demands on the materials properties of the sealant. Mechanical strength, compliance and wetting properties with the structural materials used to form the cavity for which the seal shall maintain the hermeticity over time is crucial properties.

Conformal coating – Conformal coatings main purpose is to provide a protection layer on exposed surfaces of the electronics inside the enclosure. The coatings typically have high dielectric strength which makes the suitable to prevent shorts by arcing and surface migration of the materials beneath the coating. Another benefit from using a coating is that it immobilizes the atoms on the surface of the conducting traces which inhibit electromigration in the metal core region.

The case study investigated in this project request safe handling of transient but high voltage spikes in the magnitude order of 1000-1500 V. Since the SiC BJT is only about 330 µm thick, i.e. the distance between collector and emitter, inert gases or vacuum won't do (they require at least 400 µm isolation distances for

these voltage levels). I.e. a conformal coating is required at the board level near both the transistors and diodes.

Electronic liquid – Another way to provide a dielectric protection for short circuits is to fill the hermetic cavity with an electronic liquid, i.e. a dielectric liquid. In addition to the dielectric protection, an electronic liquid also improves the thermal performance of a device by allowing heat to escape from the front side of circuit board and components more effectively than gas or vacuum. Fluorinert liquids have been used for decades but due their harmful nature, both biological and their impact on the climate (global warming), novel liquids have emerged. Solvay, 3M, Exxon all offer interesting electronic liquids. Solexis Galden PFPE and Coolanol OS-59 are perhaps the most interesting high temperature alternatives with a high flash point and a stated operation temperature above 250 °C. Lots of uncertainties arise when using electronic liquids for longer periods of time at elevated temperatures; chemical compatibility with other materials in the packages, local charge build up, pressure build up, high temperature characteristics changes, decomposition etc.

6.1 Conformal coating

SCS Parylene HT (PHT) was chosen as the conformal coating for the surface of the ceramic circuit board with all components assembled. PHT has a dielectric strength of 200 V/µm, thus approximately 8 µm is the minimum layer thickness to prevent electric breakdown for 1500 V, assuming a perfectly uniform and fault free material (as deposited). It can operate continuously at 350 °C (in air) and up to 450 °C for shorter periods. Coating may be structurally continuous for thicknesses ranging from < 1 µm up to 75 µm. Parylene HT is vapour phase deposited onto the surface which makes it ideal to get a uniform coating that cover all exposed surfaces closely without voids. It has been confirmed by the public domain that the coatings are exceptionally uniform and may cover complex structures with micron sized details in satisfactory way. A silane pre-treatment process is required to get good adhesion to Au surfaces. The adhesion to Au may be a major issue for the case study since the power module have Au as the top metallization. An experiment was planned to coat the final circuit board, with the Ni and Au, layers to qualify the coating for our design. But, since we never managed to plate this substrate, this experiment was never performed.

6.2 Base plate

6.2.1 Materials and methods

Silicon carbide reinforced aluminum, or AlSiC, is a rather novel material that combines both an attractive CTE match (< 6 ppm/K to 11 ppm/K) with a high thermal conductivity (180 W/mK to 200 W/mK). This makes it an attractive match with ceramic based electronic systems. AlSiC is typically produced through casting process. A porous SiC preform is filled with liquid Al in the casting process. This creates a component that is light weight with a pure Al surface. The Al surface may be cold spray coated with Cu, building a tens of microns thick Cu layer (e.g. for bond purposes). AlSiC is machinable and chemically stable with many common corrosive environments. AlSiC is very expensive compared to more common materials, but this is mainly due to the still low volumes requested today, according to the suppliers. Both the start-up cost, about kNOK 50-150 for tooling and design, and the part cost, NOK 500-5000, are high.

6.2.2 Results and discussion

Simulations of a simply supported stack with the Si_3N_4 ceramic substrate attached with a Cu-Sn SLID bond to an AlSiC baseplate with a 150 µm thick Cu surface layer was performed.

The simulations revealed relatively high plastic strains, (up to ~10 %) in the Cu layer at the outmost corner of the Cu / AlSiC interface.

An AlSiC-10 base plate, 220 x 92 mm^2, with three fields with a 150 µm cold spray coated Cu layer on the surface, was acquired (Figure 21). The Si_3N_4 circuit board was attached to the base plate with an adhesive (Duralco 4703). The assembly was put in an oven at 250 °C and stored there for 2700 hours (in air).

No faults or unexpected behaviour of the AlSiC base plate was observed. Cracks or delamination, suggested by the simulations, was not observed on the tested samples.

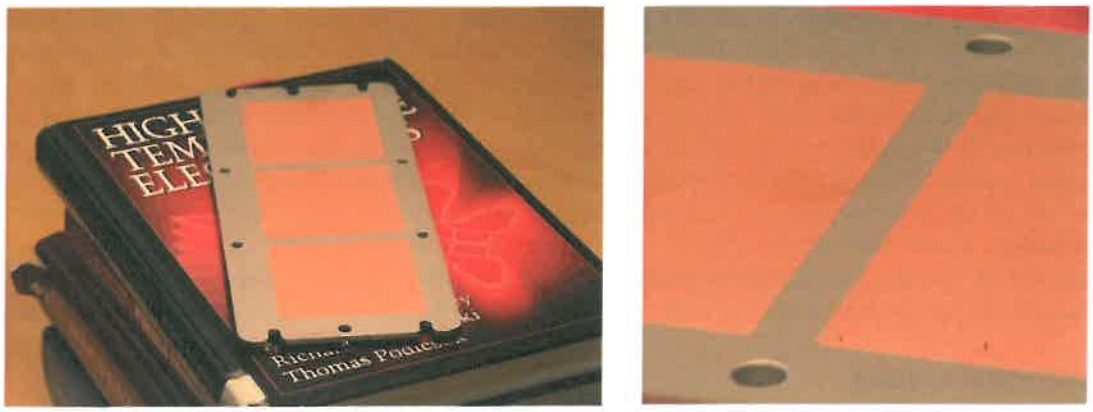


Figure 21. AlSiC base plate with 150 µm Cu top metallization.

The results regarding the AlSiC base plate are discussed in more detail in section 7.

6.3 Electronic liquid

A potentially attractive solution to improve the thermal performance of an electronic device that dissipates heat with high energy density (the SiC BJT in the case study dissipates ~1.6 MW/m^2) is cooling from both sides of the active chip. Electronic liquids provide a means to achieve this. High heat transfer coefficients may be achieved by using a liquid (up to 1000 W/m^{2}K for convection and up to 20000 W/m^{2}K by a phase change processes).

6.3.1 Results and discussion

Simulations on early concepts for the case study (Figure 22 and Figure 23) revealed that the additional need for cooling was limited for the suggested system, since the primary heat path, through die / die attach / substrate / TIM / base plate / TIM, was found to be very efficient with limited over-temperatures. Since the additional cooling performance was limited, and the added complexity by using an electronic liquid, it was not used in the final concept. For future concepts it may be reconsidered, especiall if the energy density increases significantly.

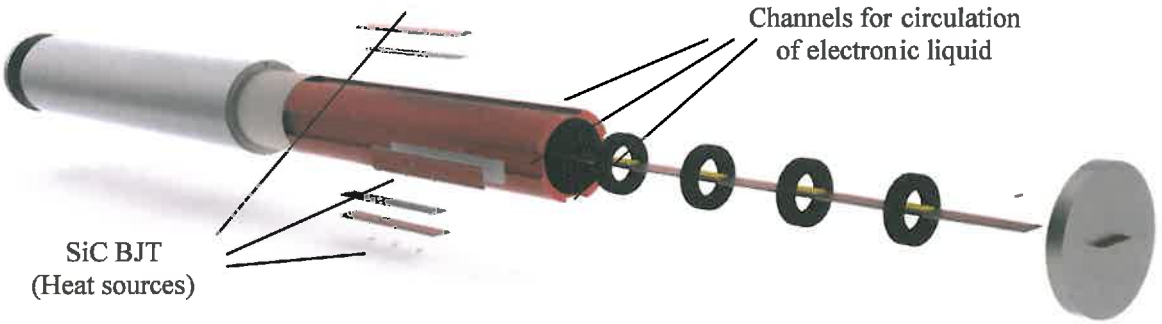


Figure 22. Illustration (exploded view) of an early concept. The concept contains integrated channels for circulation of electronic liquid flowing past the SiC BJT.

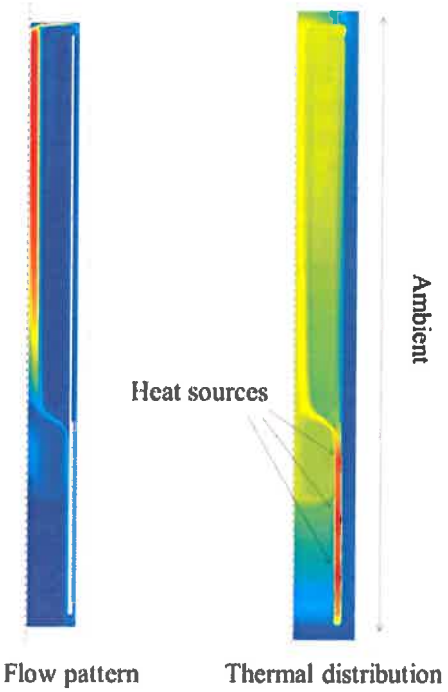


Figure 23. Flow pattern and thermal distribution for an early concept with liquid cooling (circulation of an electronic liquid by natural convection). The dashed lines indicate the symmetry axis for the 2D axisymmetric model.

7 Thermal interface materials

Different high temperature adhesives and metallic bonds were investigated regarding application as thermal interface materials (TIMs). TIMs are materials used to minimize the thermal contact resistance in the interfaces between the different layers/ levels in a package. In addition, it is sometimes used as an adhesive/ joint to secure components to one another. Important characteristics are low thermal bulk conductivity and low effective thermal resistance, i.e. the sum of the resistance due to thermal conductivity of the TIM and contact/ interface resistance between the TIM and the two contacting surfaces. The effective thermal resistance is among other things dependent of the thickness of the TIM and the actual area in which the TIM and contacting layers have mechanical contact. An overview of the different interfaces requiring TIMs in this project is given in Figure 24. Die attach is used to fix components, e.g. transistor, resistor and capacitor, to the substrate. It needs to have low thermal resistance, and in some cases it needs to be electrical conductive. The different die attach materials investigated in this project is summarized in section 4. One TIM was used to fix the substrate mechanically to a support structure (avoid screws/clamps which are known to generate unpredictable behavior (reliability) in similar systems), and ensure low thermal resistance. A second TIM was applied to minimize thermal resistance between support structure and external housing.

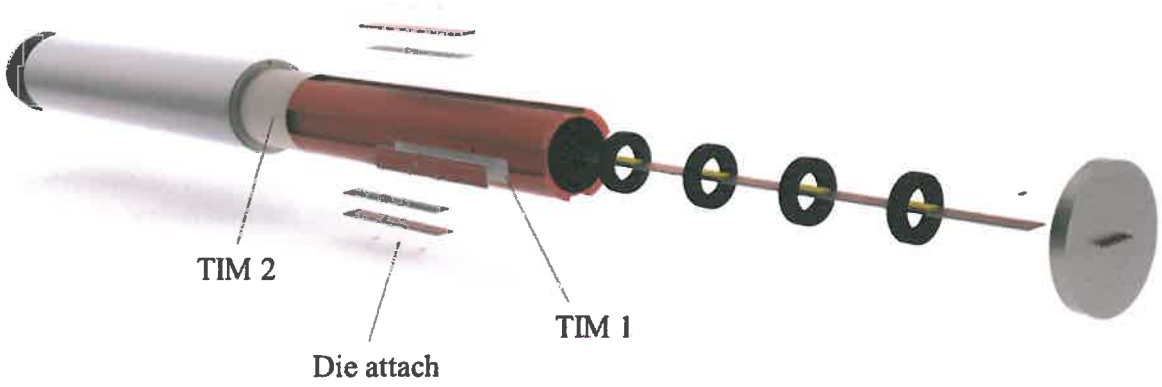


Figure 24. A schematic overview, identifying the main interfaces where a thermal interface material (TIM) is required.

7.1 High temperature Adhesives

In an adhesive used for thermal management, the mechanical strength comes from the matrix, while the particles/ material base provide the chief part of the effective thermal conductivity. Advantages with adhesives or filled polymers used as thermal interface materials (TIMs) include that they are easy to handle (relatively), conforms to surface irregularity before cure, have a low elastic modulus and excellent resistance to most chemicals and solvents. They can also easily be adjusted to the size of the mounting surfaces. Disadvantages include that curing is required, thermal conductivity is low compared to that of pure metals and delamination and adhesion (specially to Au) can be a problem in addition to thermal degradation. Delamination can be a result of the coefficient of thermal expansion (CTE) mismatch between the polymer and the fillers. This will create local stress inside the filled adhesive, possibly leading to cracks and delamination.

7.1.1 Materials and Methods

An overview of the different high temperature adhesives investigated in this project can be found in Table 4. Note that Au-Sn and Cu-Sn SLID are included for comparison.

The two most investigated adhesives were Resbond 931 and Duralco 4703. Resbond 931 is a graphite filled silica with good thermal conductivity and a high degradation temperature which is reported to give interface

thicknesses down to 100 µm. The degradation or decomposition temperature are important parameters since the decomposition of a high temperature adhesive usually only involve decomposition of the polymer. This can potentially change the properties and reduce the reliability of the adhesive, since the polymer provides the mechanical strength. Outgassing, which is closely connected to degradation, is also an important parameter. The outgassing of Resbond 931 is relatively low at 300 °C compared to the intended operation temperature of the case study (200 to 250 °C).

Duralco 4703 is an epoxy filled with Al_2O_3 powder. It offers high temperature stability (degradation temperature of 330 °C), has excellent resistance to most chemicals and is easily handled. The interface thickness of a Duralco 4703 bond can be made very thin, giving low effective thermal resistance.

An overview of the different substrates and chips/ bricks used to test the different adhesives can be found in Table 5. Before assembly, the substrates and chips/bricks were cleaned with acetone, isopropanol and dried with nitrogen. All the tested adhesives were mixed, applied and cured according to the data sheets provided by the different suppliers.
After assembly the samples were characterized with shear testing (in a Dage 2400A or NordsonDage 4000plus) and by optical microscopy. Some samples were cross-sectioned and inspected by optical microscopy.

Selected samples were stored at high temperature (HTS), at 250 °C, for 2600 hours. The samples were visually inspected once a week to check for obvious degradation, such as catastrophic mechanical failure by detached substrates from the base plate.

Table 4. Overview of different thermal interface materials investigated.

Name	Material base	Effective thermal conductivity (W/m·K)	Degradation temperature (°C)	Outgassing @ 300 °C	Expected final layer thickness (µm)	Estimated thermal resistance[3] (mm^2·K/W)
Au-Sn SLID	Gold and tin	60	T_m: 522	-	~10	~0.17
Cu-Sn SLID	Copper and tin	104	T_m: 676	-	<10	<0.10
Duralco 4703	Epoxy with Al_2O_3 powder	2.55	330	0.33%	~50	~20
Epo-tek 353ND	Epoxy	0.10-0.15	412	0.87%	~4-6	~40
Resbond 906	Silicate with magnesia	5.6	1650	Low	~100	~17.9
Resbond 931	Silicate with graphite	8	3000	-	~100	~12.5
Resbond 954	Silicate with stainless	>2	1200	Low	~100	~50
Staystik® 581	Silver	>3	300	Low	38	12.7

Table 5. Overview of the different substrates and chips used for the different adhesives tested. The measured shear strength is also included where applicable.

Substrate	Chip/ brick	Adhesive	Shear strength (MPa)
Cu / Ni plated Si_3N_4 (6 x 6 mm^2)	Au plated Cu (3 x 3 mm^2)	Resbond 906 Resbond 931 Durabond 954	NA NA NA
Cu / Ni plated Si_3N_4 (6 x 6 mm^2)	Cu (3 x 3 mm^2)	Resbond 906 Resbond 931	1.3 3.4
Cu plated Si_3N_4 (6 x 6 mm^2)	Cu (3 x 3 mm^2)	Resbond 931 Epo-tek 353ND Staystik 581 Duralco 4703	6-7 7 NA 29
Cu plated Si_3N_4 (6 x 6 mm^2)	Ceramic resistor (Vishay PHT 2010)	Duralco 4703	21
AlSiC baseplate (see Figure 25)	Cu plated Si_3N_4 (6 x 6 mm^2)	Duralco 4703	NA: Not possible to shear of the substrate due to large bond area

Table 6. Overview of the TIM systems exposed for HTS. The measured shear strength is also included where applicable.

Substrate	Chip/ brick	Adhesive	Shear strength (MPa)
Cu plated Si_3N_4 (6 x 6 mm^2)	Ceramic resistor	Duralco 4703	4
AlSiC baseplate	Cu plated Si_3N_4 (6 x 6 mm^2)	Duralco 4703	-

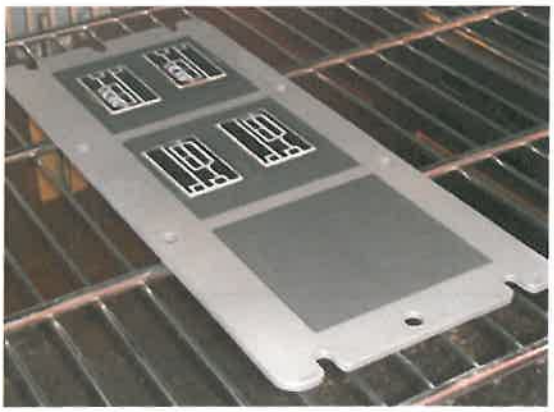
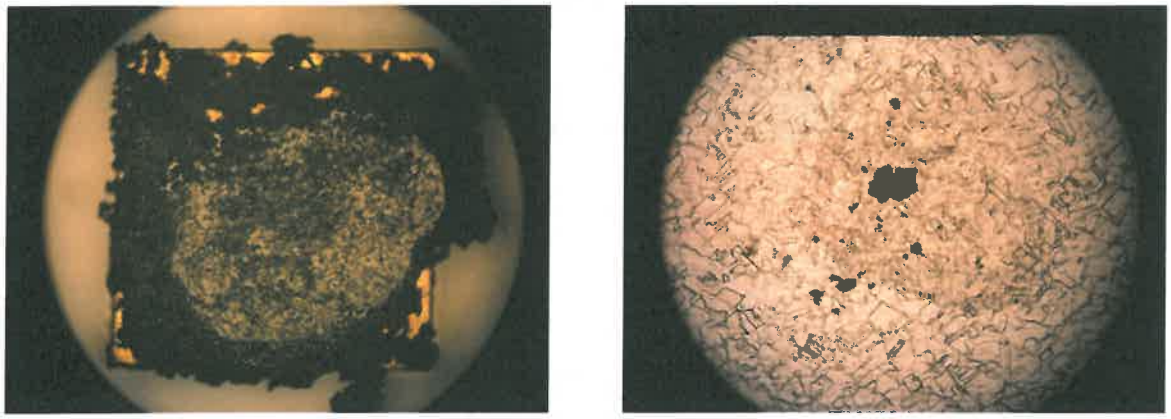


Figure 25. Si_3N_4 substrates glued to an AlSiC baseplate with Duralco 4703. Two of the substrates contains three (six in total) Vishay PHT 2010 resistors glued with the same Duralco 4703.

7.1.2 Results and discussion

All samples glued with Resbond 906, Resbond 954 and Staystik 581 failed before shear testing or cross-sectioning. The main reason for this was poor adhesion. A typical fracture surface is shown in Figure 26. This image is also representative for the other fractures.



(a) (b)

Figure 26. Fracture surfaces of samples bonded with Resbond 954.

After some process optimization, acceptable adhesion was achieved with Resbond 931, ~6 MPa. However, the interface was quite thick, ~200µm, and the adhesive was very difficult to work with.

A sufficient adhesion was also realized with Epo-tek 353ND (~7 MPa). This adhesive was ok to work with/ handle, and it was possible to obtain a thin joint. However, as can be seen below, Duralco 4703 had more appealing properties, and was therefore further investigated.

The most promising high temperature adhesive investigated was Duralco 4703. The shear strength was high (~30 MPa for Cu-Cu adhesion and ~20 MPa for Cu-ceramic resistor adhesion), the interface was thin and void free, (~50 µm, see cross-section in Figure 27), while it was easy to work with. However, after high temperature storage, the shear strength was greatly reduced to only ~4 MPa. It should here be noted that the high temperature stored samples experienced some thermal cycling during the storage period, due to power failure in the lab. The reason for the large degradation of shear strength is unknown. One possible explanation could be thermal degradation of the polymer material during high temperature storage.

The Cu-plated Si_3N_4 substrates bonded with Duralco 4703 to the Cu-plated AlSiC baseplate failed during high temperature storage. An image of the fracture surfaces is shown in Figure 28. The reason for this failure is unknown. As for the above mentioned sample, the reason could be thermal degradation of the polymer material during high temperature storage. This can be a plausible reason, since all samples looked ok during the visual inspection only two weeks prior to the failure. If there was degradation, the degradation rate should be more or less comparable for all samples, giving a spontaneous failure of all tested samples as was observed.

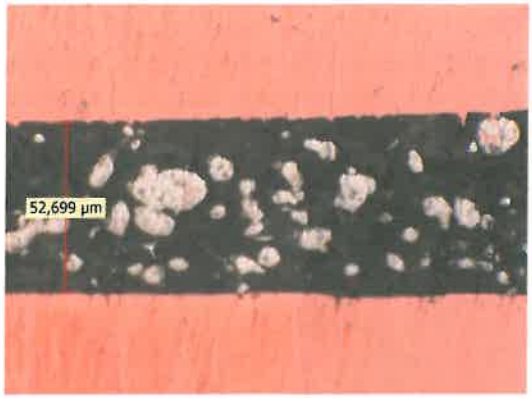


Figure 27. Cross-section of a Duralco 4703 sample.

Figure 28. Image of the fracture surfaces of a Cu-plated Si_3N_4 substrate bonded to a Cu-plated AlSiC baseplate after thermal aging (2600 hours at 250 °C).

7.2 Metallic thermal interface materials (TIMs)

The main advantage by using a metal compared to an adhesive for thermal interface materials (TIMs) is that the metal has much higher thermal conductivity. That combined with a thin joint give a lower thermal resistance of the joint than the polymer based adhesives (see Table 4). However, metals are in general harder (sometimes brittle) than polymers, leading to challenges regarding stress induced from e.g. CTE mismatches. Other challenges are associated to the requirements of surface roughness and intermetallic diffusion. A metallic TIM requires much more uniform contact surfaces than e.g. adhesives. Intermetallic diffusion will often create brittle and unreliable interfaces, especially during high temperature exposure. More about intermetallic diffusion can be found in section 4.

7.2.1 Materials and methods

NanoFoil

RNT's patented NanoFoil® is fabricated by vapour depositing thousands of alternating nanoscale layers of aluminum (Al) and nickel (Ni), the total foil thickness ranges from 40 – 80 µm. When activated by a small pulse of energy from electrical, optical or thermal sources, the Al-Ni layers react exothermally. The foil creates a self-sustaining reaction that acts as a rapid and controllable localized heat source to melt adjoining solder layers, bonding components together. In contrast to normal soldering the process can be carried out at room temperature. After reaction, the Al and Ni layers forms an Al-Ni alloy.

In this project Nanofoil bonding using a 40 µm thick NanoFoil was examined in a package consisting of two Si_3N_4 (6 x 6 mm^2) substrates with copper / Ni /Au metallization. 25 µm thick Au-Sn preform from Indium Corporation was used as soldering material (see Figure 29). A force (two clamps corresponding to a pressure of 6 MPa on the bonded surfaces) was applied to assure sufficient contact between the bonding surfaces, while a 9 Volt battery was used for ignition of the nano-foil.

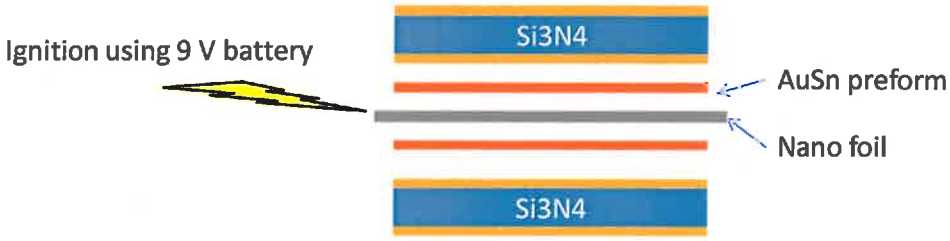


Figure 29. Stack for NanoFoil bonding.

Cu-Sn solid-liquid interdiffusion (SLID)

Cu-Sn solid-liquid interdiffusion (SLID) is similar to Au-Sn SLID (cf. section 4) regarding the methodology by producing a high melting point intermetallic compound from a bi-metal sandwich structure including a low melting point material. Thus, a low process temperature, about 300 °C, creates a bond with a melting temperature of 676 °C (for the Cu-Sn system). Its homologous temperature at 200 °C is ~0.5, which indicates that it is a suitable candidate as a high temperature compatible thermal interface material (TIM). Since the SLID process consists of a liquid phase during the bond process, cf. Figure 6, rough surfaces are bondable which should make the SLID process feasible for larger joints, such as a TIM for the back side of the substrate. Regarding Cu-Sn joints, care should be taken. Unless the process is optimized Cu-Sn bonds may easily hold poor quality, with micro voids and oxidation formation. The final Cu-Sn phase, ε (Cu_3Sn), is also harder (brittle) than the Au-Sn phases, ζ and β, hence the stress distribution in a potential bond must be evaluated in an initial feasibility study.

Simulations of the ceramic substrate attached with a Cu-Sn solid-liquid interdiffusion (SLID) bond onto the AlSiC-10 base plate was investigated to evaluate the feasibility for utilization of a metallic thermal interface on the substrate back side. The metal bond has superior thermal properties compared to regular thermal adhesives. The main drawbacks for large metallic bonds, here with a characteristic length of ~40 mm, are limited fatigue life and its creep resistance, both due to thermo-mechanical induced stress at high temperatures.

7.2.2 Results and discussion

NanoFoil

Several bonding trials were performed. By preheating the stack to 200 °C prior to bonding, ok results were achieved, but only partly bonding was obtained (~50-70 %). The shear strength was measured to ~10 – 14 MPa. The reason for the partial bonding might have been due to insufficient bonding pressure, giving air gaps, or pockets, in the stack. These pockets would give non-uniform temperatures in the stack during bonding, preventing complete melting of the Au-Sn preform/solder. Or they might prevent melted solder on each side of the pockets to get in physical contact with each other. By increasing the bonding pressure in combination with preheating to a higher temperature, e.g. 250 °C, this problem may be solved. A cross-section of a typical bonded sample is shown in Figure 30. Electron dispersive spectroscopy (EDS) revealed that very complex intermetallic compounds (IMCs) were created in the bonding process. There was a combination of Al-Au-Ni-Sn IMCs, and since the resulting Ni-Sn IMCs are known to be brittle, NanoFoil was not believed to be a suitable candidate as a TIM material in the HTPEP project.

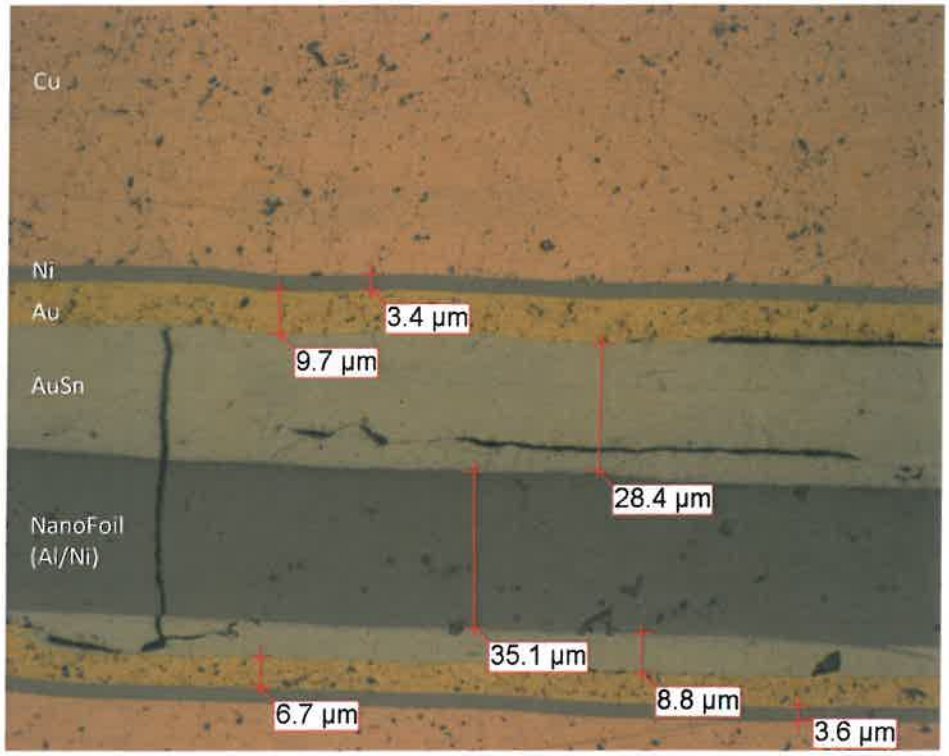


Figure 30. Cross-section of a typical sample bonded with NanoFoil.

Cu-Sn solid-liquid interdiffusion (SLID)

The thermal resistance column in Table 4 suggest a relative thermal performance gain by exchanging a typical high temperature adhesive, a particle loaded epoxy (Duralco 4703), with a Cu-Sn bond. A global thermal analysis of the concept, developed for the case study, was performed. It investigated the potential performance gain. The boundary conditions that were used are presented in Figure 31 and Figure 32. The boundary conditions shown in Figure 31 were estimated to represent downhole application conditions. The results showed that the heat generation is localized to the SiC BJT with only a limited effective heat spreading (laterally inside the substrate), see Figure 33. This is due to the efficient thermal path beneath the transistors. A study of the temperature profile from the SiC BJT to ambient showed that it was primarily the substrate, the thermal interface material between the substrate and base plate and the heat transfer to ambient that contributed to the over-temperature of the device (Figure 34 and Figure 35). The study also showed that the maximum over-temperature of the transistors could be reduced by 5 to 10 °C by replacing the epoxy with the metallic Cu-Sn joint as the back side TIM. As a rule of thumb, often referred to, says; *a reduction of 10 °C of the operation temperature may double the mean time to failure (MTTF) for highly stressed systems.* This statement shall be handled with care since this is individual for every system, but it gives an impression for how important a few degrees may be for a system.

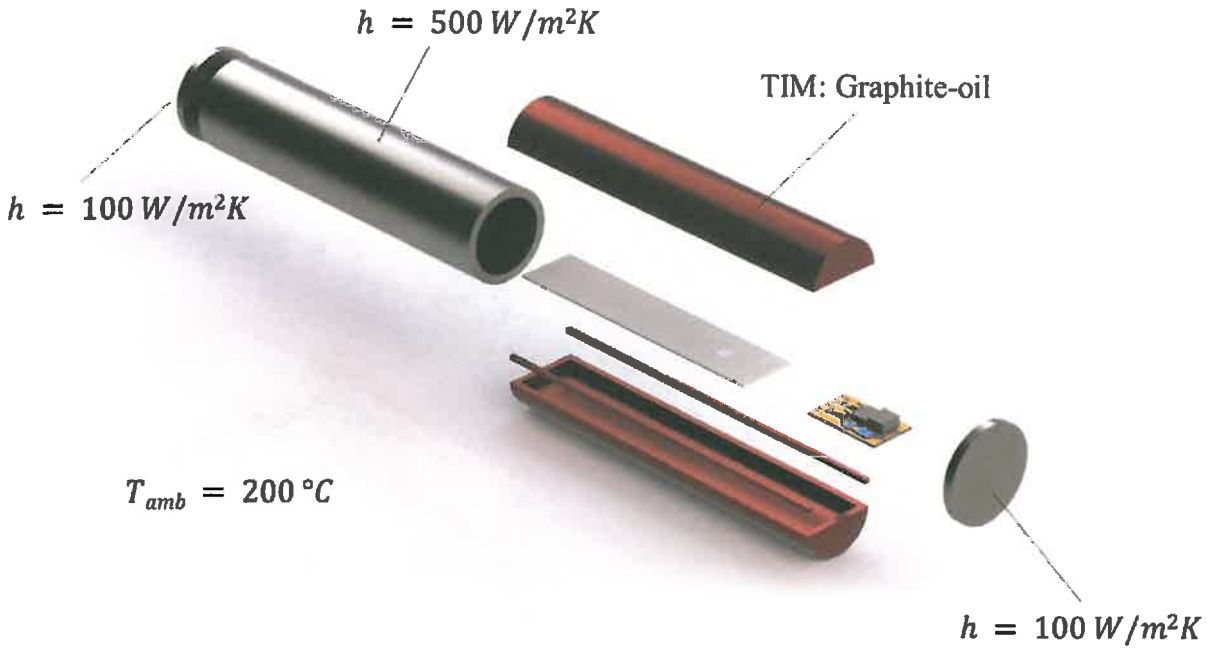


Figure 31. Boundary conditions (BC) used for the global thermal analysis of the case study (exploded view).

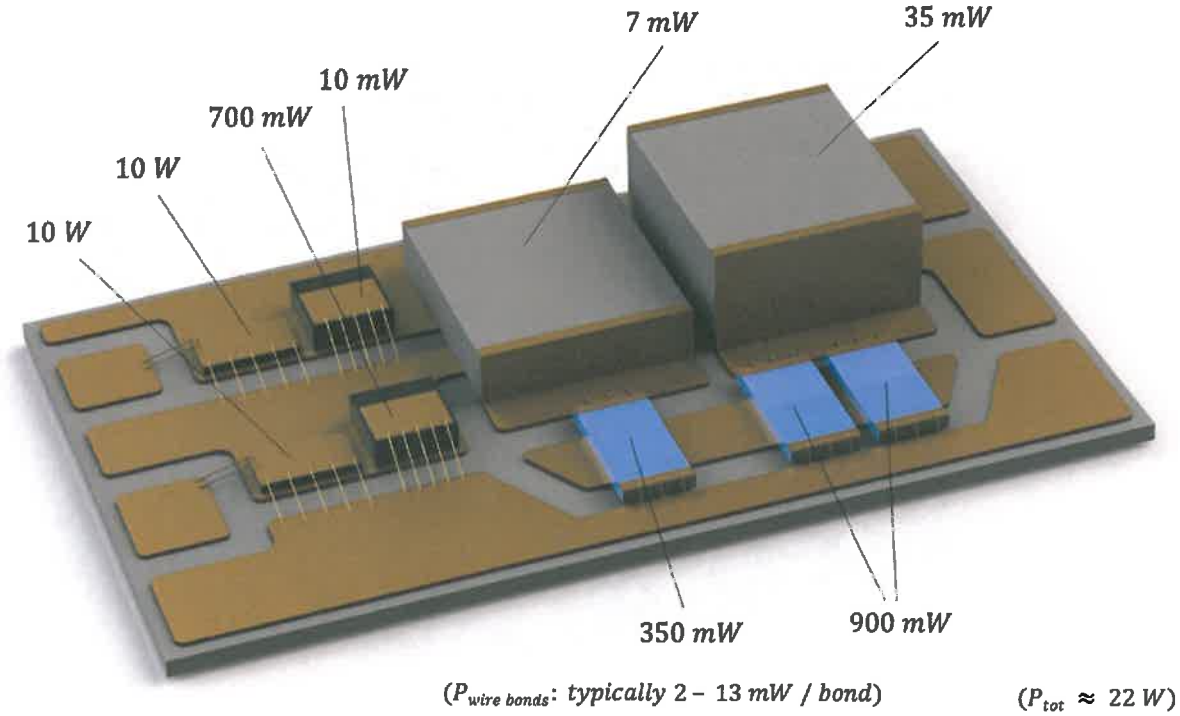


Figure 32. Dissipated power for all components on power module for the case study. The numbers were based on estimations from simulations (with SPICE) on the electronic system.

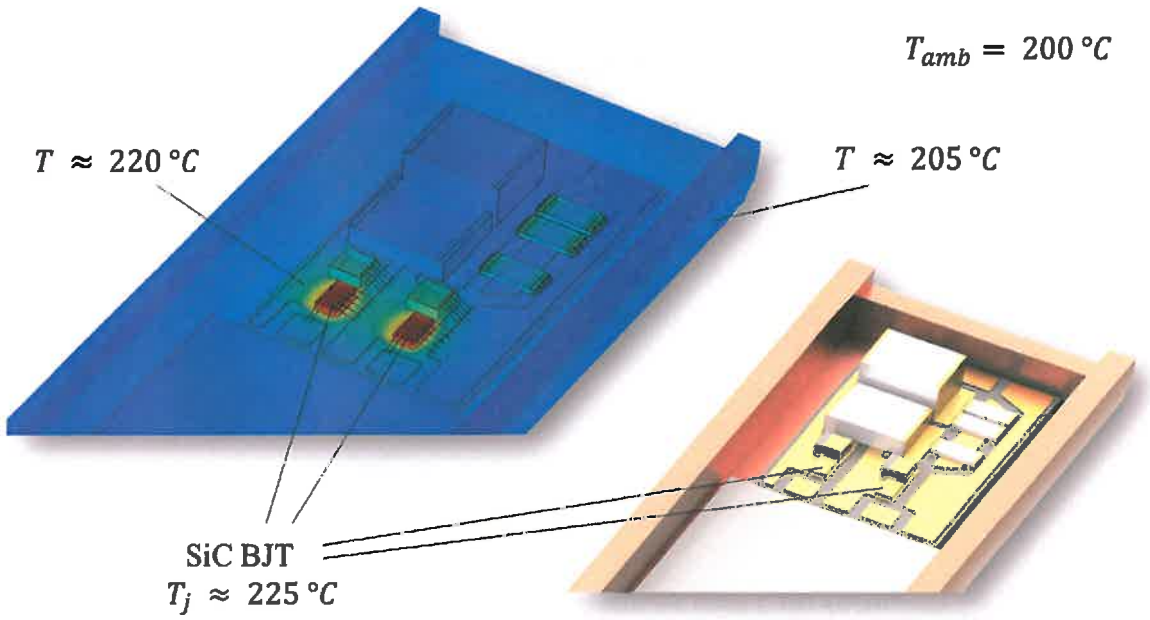


Figure 33. Resulting temperature distribution for the investigated case study.

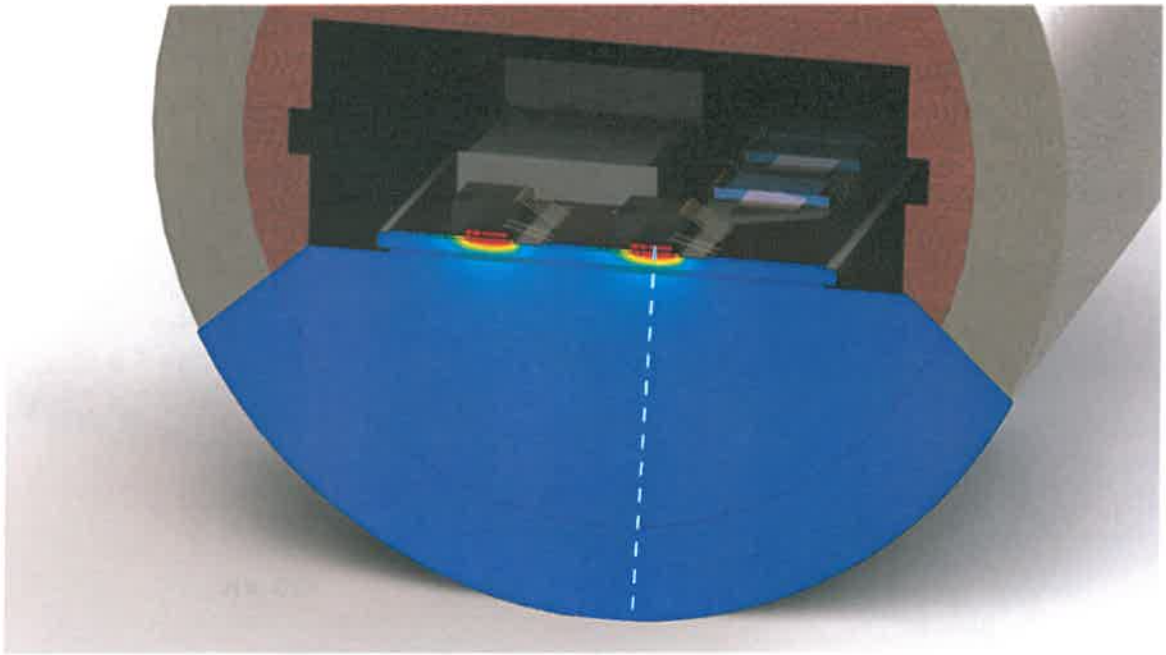


Figure 34. Illustration of the cross-section of the analysed case study. The dashed line indicates the path of the temperature drop presented in Figure 35.

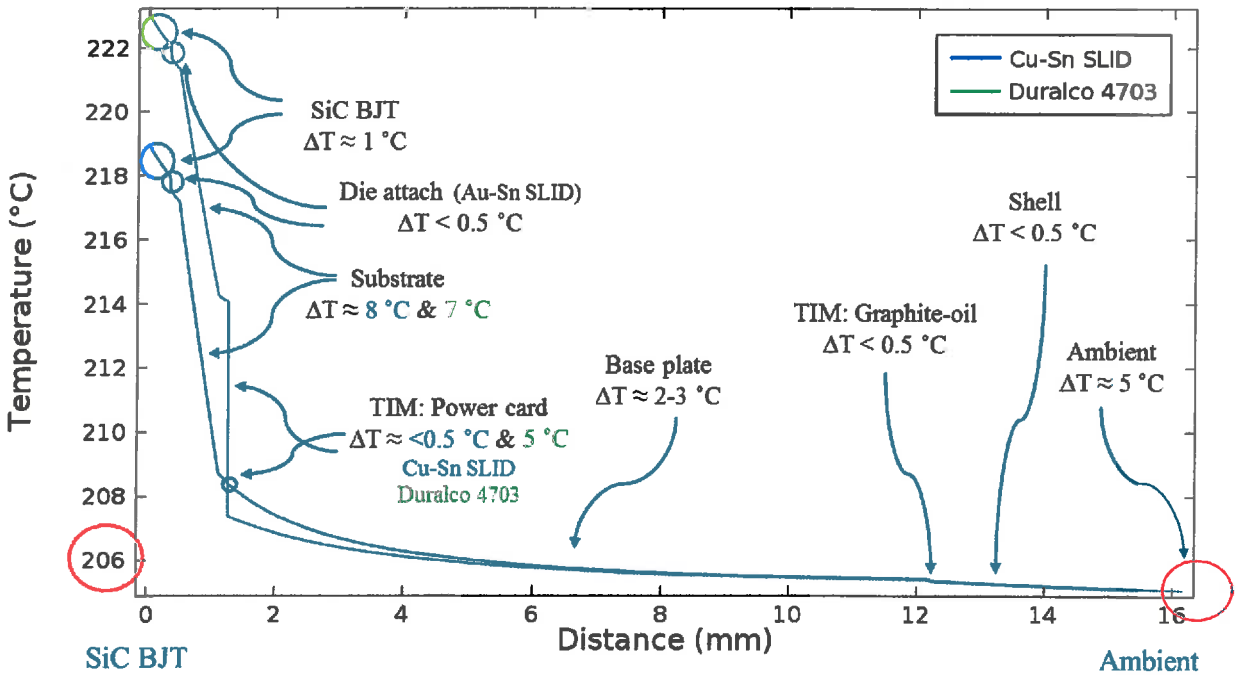


Figure 35. Temperature drop, through the case study material stack, from the surface of the SiC BJT to the ambient for the path defined in Figure 34.

Simulations of strain and deformation of a simply supported stack with the Si_3N_4 ceramic substrate attached with a Cu-Sn SLID bond to an AlSiC baseplate with a 150 µm thick Cu surface layer, see Figure 36, was also performed. Two cases, B and C, were investigated (cf. section 0 and Figure 37). Case B represents the bond process followed by cooling down to room temperature. Case C represents conditions during normal operation. The simulations revealed warpage of the entire stack, up to ~200 µm peak-to-peak, generating small plastic strain, < 1%, inside the Cu_3Sn layer and up to ~20 % in the adjacent Cu layers (Figure 5, Figure 38 and Figure 39).

Figure 36. Illustration of the power module assembled onto an AlSiC base plate for case B and C.

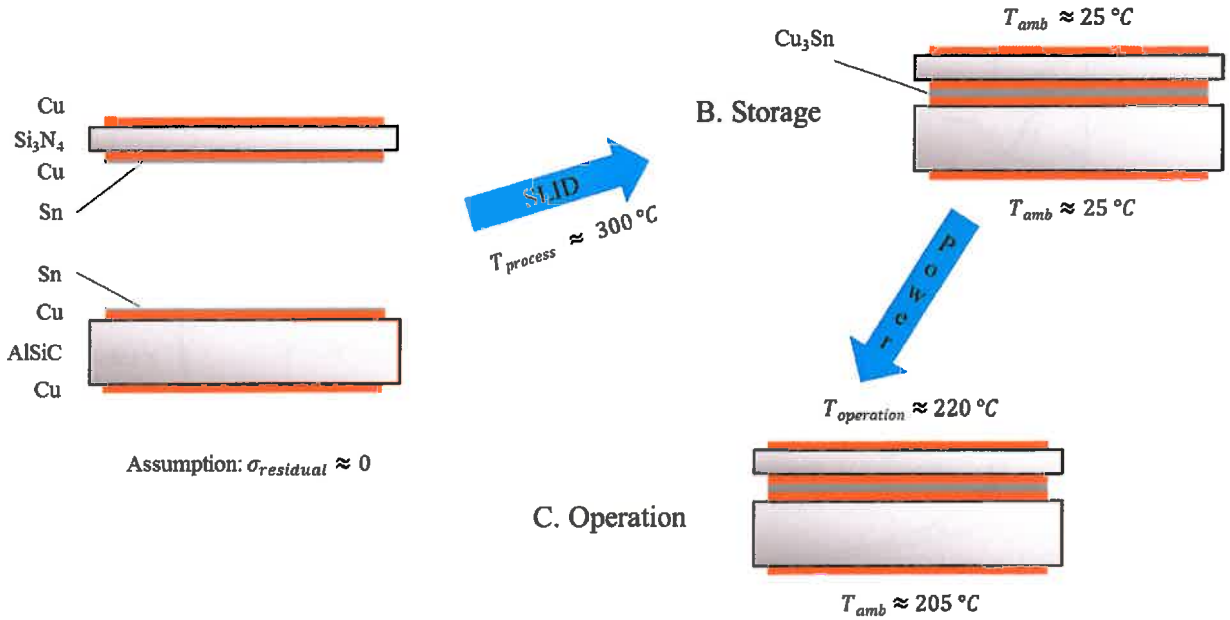


Figure 37. Illustration of the cases studied for a Cu-Sn SLID bond as potential TIM.

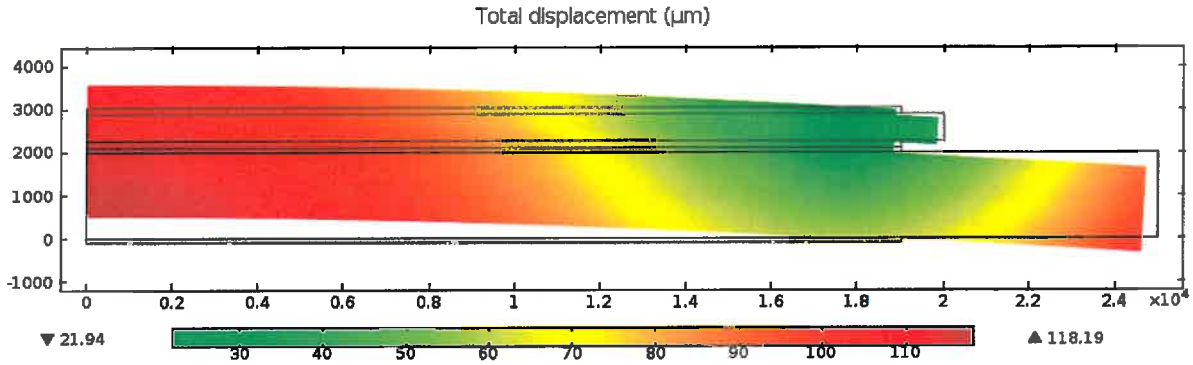


Figure 38. Resulting deformation for case B in Figure 37.

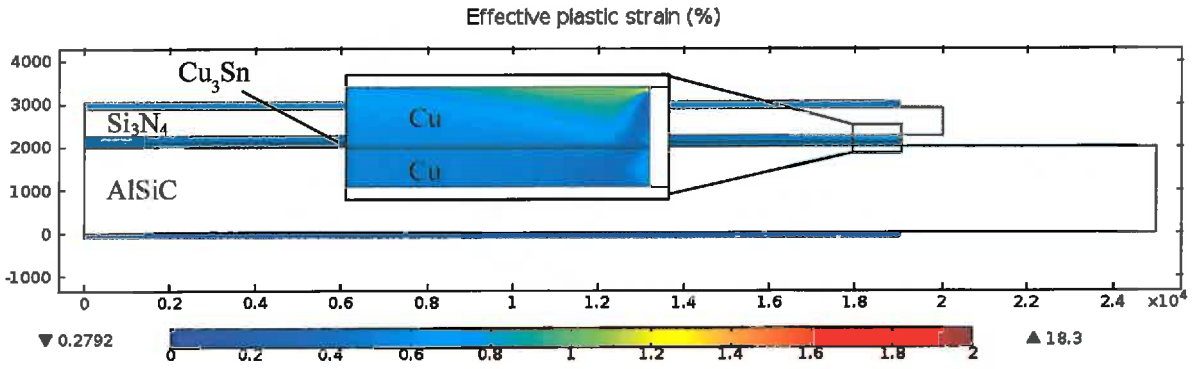


Figure 39. Effective plastic strain inside the metal layers at room temperature after a Cu-Sn SLID bond process (case C).

For all simulations incorporating the Si_3N_4 substrate the thermal conductivity was conservatively set to 60 W/mK, despite the stated 90 W/mK in the data sheet. The available scientific literature at time of analysis indicated a maximum of 60 W/mK. Recent publications have revealed numbers as high as ~100 W/mK which make all thermo-mechanical results presented in this report somewhat conservative.

8 Case study electronics

In order to design high performance power electronics for high temperature oil well operation, several disciplines must be combined. The performance depends on thermal properties as well as mechanical layout and reliability of all parts under high vibrational and shock impacts. All of these tasks must be combined with the electronic functionality in itself. Finally, suitable electronic components that will fit the requirements needed must be found.

The HTPEP project addresses all these issues and the Case study was defined in order to be a practical test bench for the individual discipline oriented studies.

Most of the work related to the case study is therefore reported in earlier chapters dealing with these studies. This chapter describes the electronics activity within the case study.

The goal of the electronics phase of the case study was to design, manufacture and test a power module (or power driver) based on silicon carbide transistors from TranSiC.

The power module, which in principle is a transistor based circuit that can connect power to a load at specific times. A single power driver is either a low side or a high side driver, depending on whether the transistor is between the load and ground or between the load and high voltage, respectively. Two drivers form a half bridge. Two half bridges form a full bridge and three half bridges form a three phase driver.

It was decided to make a half bridge as this the fundamental switching unit. The final circuit design is shown in Figure 40

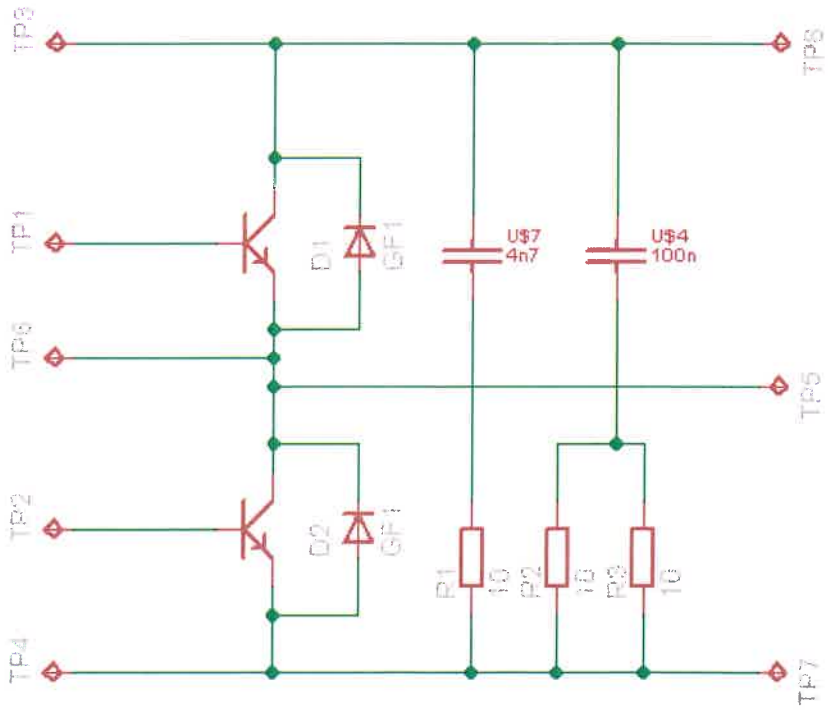


Figure 40. Circuit diagram for the power module showing transistors, diodes and snubber network.

8.1 Silicon carbide transistors

Silicon carbide (SiC) transistors has properties that are well suited for high temperature power switch applications. They will operate up to high temperatures and switch very fast and therefore opens for low switching losses. The switching losses come from two parts: A transient part when the transistor switches

from off to on state or vise versa. The second part comes from the on state at which a small voltage, V_{on}, is sustained over the transistor while the on current, I_o, flows through the transistor. The second part must be present during operation to function properly. But, to avoid unnecessary high losses, it is important to minimize the transient part, e.g. by fast switching. SiC also has a high thermal conductivity

SiC has, however, been afflicted with defects preventing its commercialization. At the time the HTPEP project was defined, a large activity on improving this situation was going on world wide. We assumed that a break through was approaching and decided to go for this technology.

An important issue was to find a partner open for cooperation on this issue and we were happy to get in contact with a Swedish company TranSiC. They had developed a SiC junction power transistor suitable for fast switching. Other companies were working on developing FET and MOSFET devices but no devices were commercially available.

By choosing the TranSiC device we got both development data at a very early stage and had excellent communication through the whole project phase.

During later years the range and availability of commercial components has improved considerably.

8.2 Circuit topology and partitioning

The power driver test case was intended to mimic a motor driver as best as possible while keeping development costs down. Typically a downhole motor needs a three phase driver in order to operate, meaning that three half bridges would have to be made to the same specifications, effectively trebling the costs of one half bridge whilst not providing tree times the knowledge. Therefore it was decided that a single half bridge would be built and tested. The performance figure for a three phase driver could be extrapolated through simulation at a later date if one should wish.

Testing a non-optimised half bridge for power switching is inherently difficult due to the high power available and the sensitive timing needed to prevent catastrophic and immediate circuit or component failure. Therefore the driver was developed and tested largely as a single low side or high side driver. The low side driver is easier to switch because it is referenced to ground, whereas the high side is referenced to the low side collector. This means that the high side needs galvanically isolated signals and power supplies. Hence the strategy was to focus on the low side first and later expand to high side. A block diagram of a half bridge topology is shown in Figure 41.

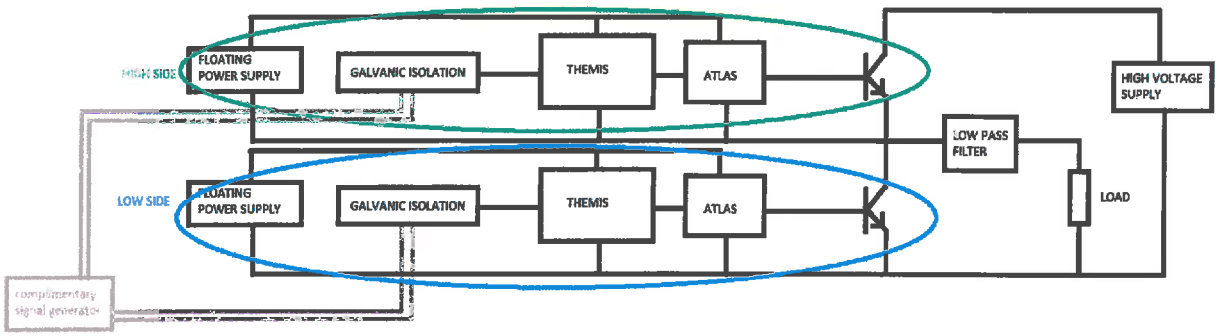


Figure 41. Block schematic diagram of a half bridge driver with load.

Due to limited component availability and cost in general it was found that only the power module needed to be made for high temperature operation, and the transistor base drivers could be kept at a lower ambient temperature. The signalling boards at the lower temperature (<175 °C) still allowing for regular components to be used, reducing costs and increased the component availability. An illustration of the sectioning of the case study setup is shown in Figure 42.

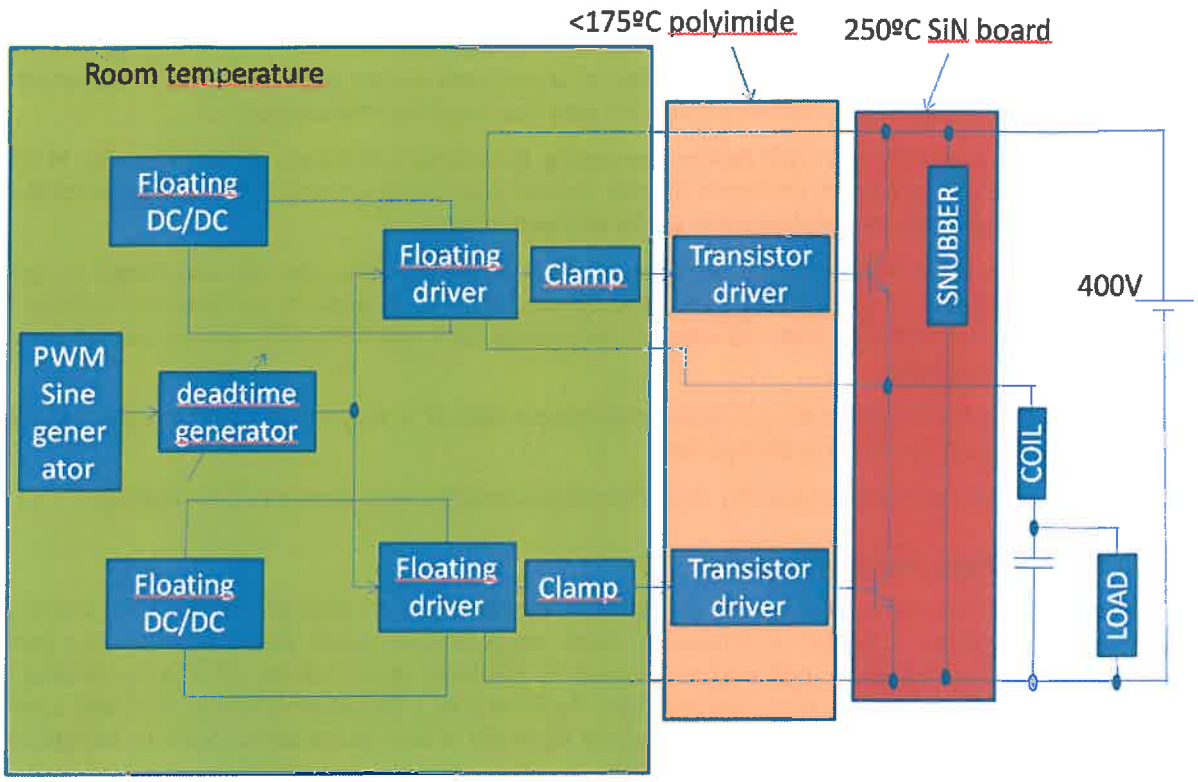


Figure 42. Circuit partitioning.

8.3 Driving a power silicon carbide bipolar transistor

The HTPEP case study chose to use SiC BJTs because they promised the lowest switching losses of all available transistors and they offer operation up to 550 °C. However, they are arguably the hardest to drive because of the high base current needed for fast switching.

The current amplification, h_{Fe}, is a key parameter, and is the ratio of output collector current to input base current. Typically this may be in the region of 20 to 35 but the transistors need about 50% overdrive in order to switch fast. The maximum load current was estimated to 6 A. Thus, a drive current of 450 mA was requested.

In order to switch the BJT as fast as possible it is best to give the initial base current an extra "kick" in the start, and in our case it can reach several amperes for some nanoseconds. This will flood the base with free carriers, sending the transistor into full saturation. The 50% overdrive will keep it in full saturation (minimum collector-emitter voltage). When it's time to turn the transistor off the free carriers must be removed as fast as possible. In order to ensure the fastest turn-off we therefore need to apply a negative base current, attracting the free base carriers to exit back through the base instead of travelling across the junction to the collector.

8.3.1 The CISSOID driver

Originally both the power module and base driver were intended to run at high ambient temperatures (200-250 °C) for at least 6 months. In order to achieve this reliably one has to use either bare die components or components made specifically for such high temperatures.

Extensive effort was put in in order to evaluate different technologies that could be suitable. From the onset, the company CISSOID claimed to have a suitable solution for high temperature in their "soon-to-be-

launched" product series. A lot of effort was put into trying to make their chipset work, but eventually the chipset was found to be somewhat unreliable and self-destructive. Ultimately the design was left for a simpler solution with more discrete components. The simplified design required though that the base driver was kept at a lower temperature (<175 °C) than the power module.

Their soon-to-be-launched HADES chipset included ATLAS and THEMIS (Figure 43), a chipset promised a scalable driver solution that should be usable for MOSFETs, IGBTs and even BJTs.

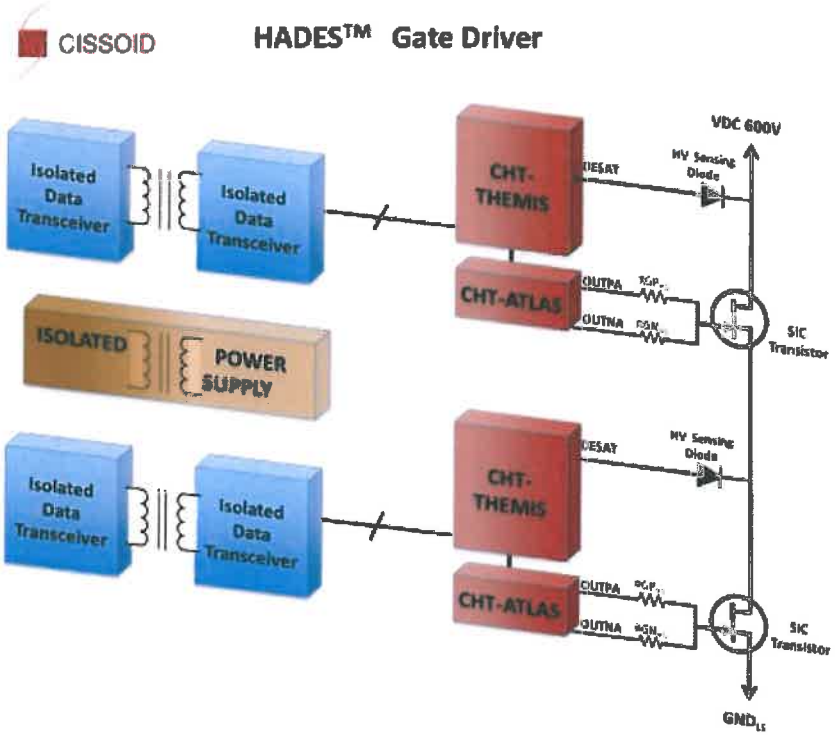


Figure 43. CISSOID's HADES driver consists of many chips, including the THEMIS and ATLAS chipsets.

The other parts were an isolated signal transceiver called RHEA and a floating power supply called STROMBOLI. All parts were available as plastic packaged components for operation up to 175 °C and as bare die and ceramic up to 225 °C and beyond.

The THEMIS is a logic chip that controls and supervises the power transistor driver ATLAS. The THEMIS offers 50 ns turn/on and turn/off times as well as circuit protection. The ATLAS has two channels, each capable of driving 2 A. They can be paralleled through 1 Ω resistors. This should provide sufficient drive for the BJTs but there was no guarantee.

The chips themselves are very complicated and required many surrounding parts (cf. Figure 44). Furthermore the components were very expensive (several hundred euros each) and with high minimum orders for bare die there was no guarantee that the project could afford to opt for a bare die solution. Nevertheless it was the best option at the time.

Extensive effort was put into building and testing the THEMIS + ATLAS chipset in accordance to CISSOID's recommendations and advice. Figure 44 show the schematic circuit diagram for a half bridge based on the CISSOID chipset.

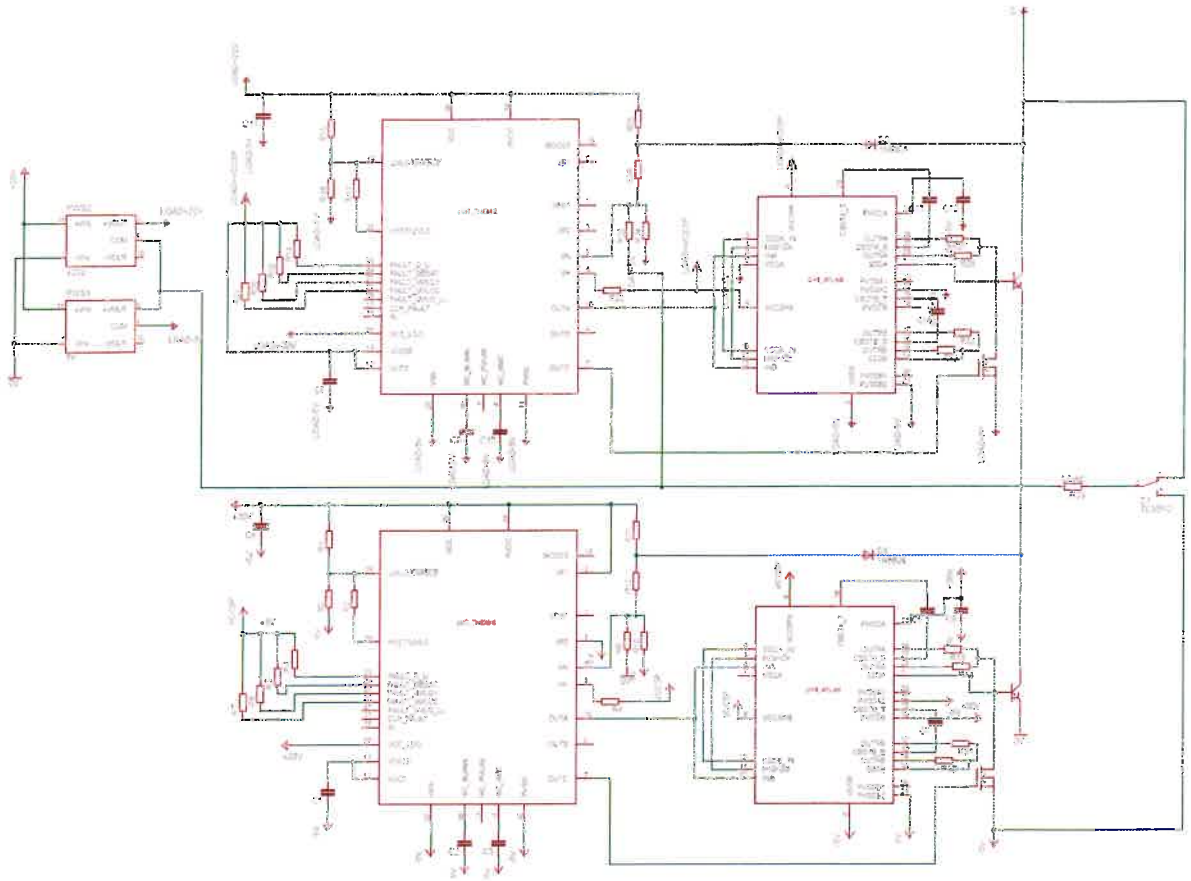


Figure 44. CISSOID chipset based half bridge driver with surrounding parts.

Simulations on the CISSOID driver were performed (Figure 45). The driver was modelled as an ideal source with adjustable rise and fall times, on and off voltage and a 2 Ω resistance for the two gate driver channels.

R28 and R35 represent the internal ATLAS driver resistances. R34 and R36 were physical resistances outside the ATLAS chip. The resistor/ capacitor network included stray inductance in the R27 and R25. R27 was sown to dissipate roughly 2 W and was therefore made up of 4 parallel resistors which could dissipate 0.5 W each.

The transistor package stray inductance was included in the simulations. These values would change if the design would evolve into a bare die version, for better or worse.

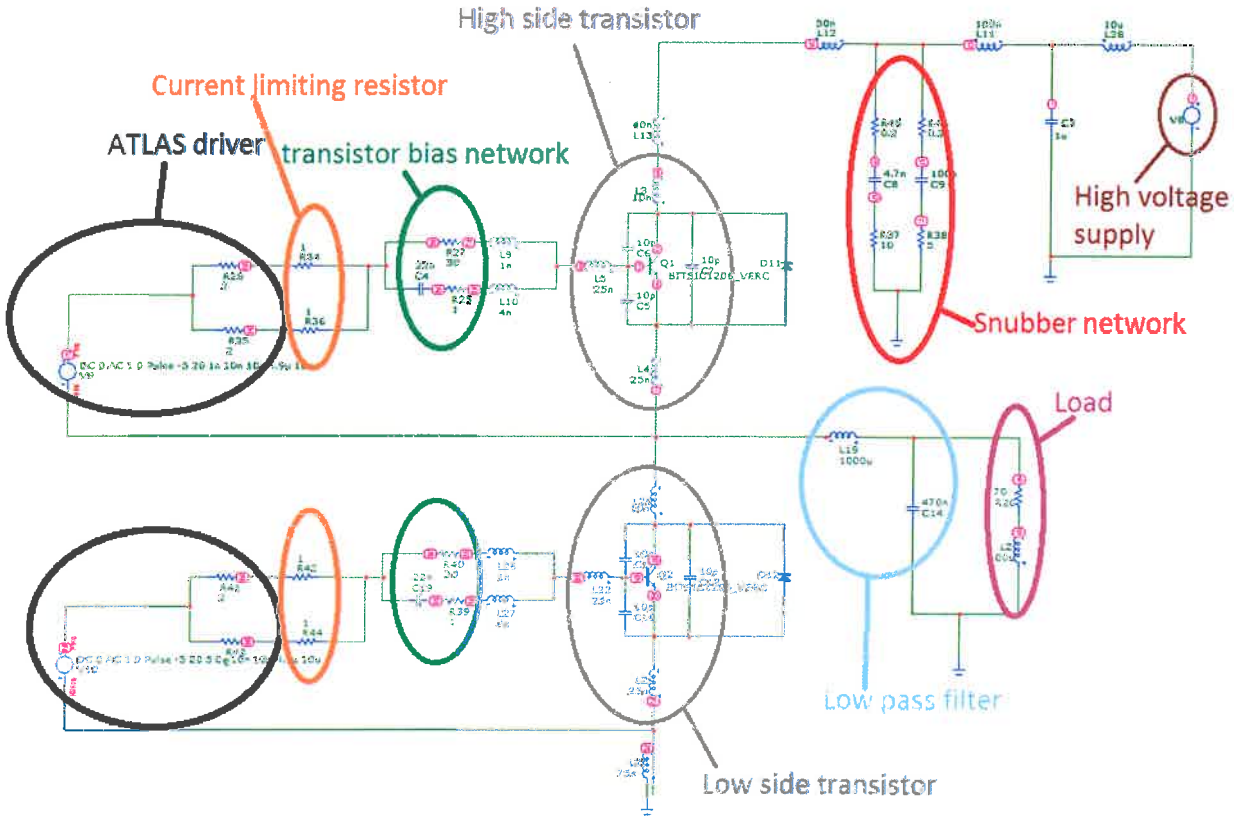


Figure 45. CISSOID chipset based half bridge driver simulation diagram.

The simulation indicated that the drive circuit would deliver 220 mW, which was well within specifications. Base current would initially be 3.7 A and then settle to 275 mA (Beta, or h_{FE} was set to 20). Note that the 3.7 A initial peak base current is at the limit of what the ATLAS chips are specified to deliver.

Figure 46 shows the simulated estimate of the average power dissipated in a single BitSiC 1206 running at 400 V, with a load of 100 Ω + 400 µH. The switching frequency was 200 kHz.

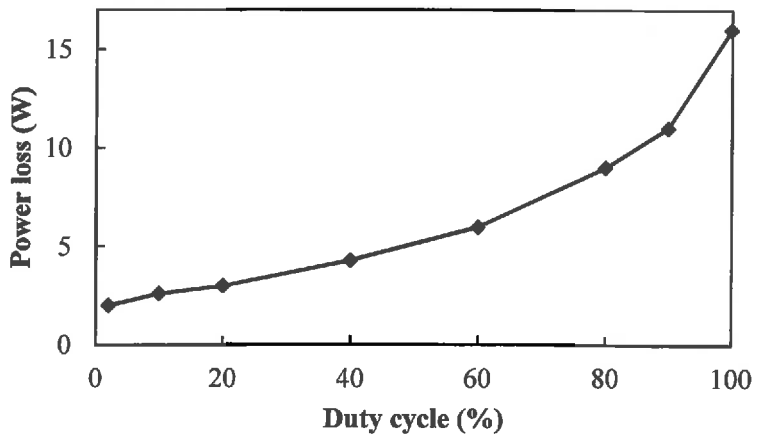


Figure 46. Simulated power loss versus duty cycle.

As can be seen in Figure 46 the power reaches up to 16 W for a duty cycle approaching 100%.

If another BJT is added to the RC network, it is possible to distribute the load current and thereby reduce the power dissipated per transistor. Thermal performance simulations showed that this was not necessary to keep the junction temperature below 250 °C (cf. section 7). But it should be kept in mind as an option, e.g. if additional life time of the package is requested.

Based on the simulation results a test board was designed and built as a single driver, see Figure 47 and Figure 48.

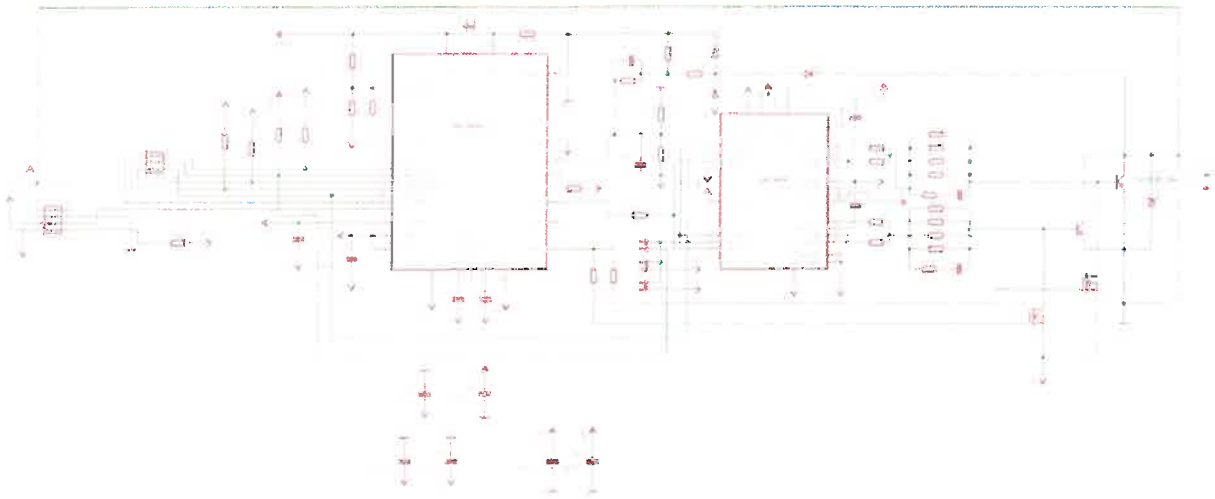


Figure 47. CISSOID base driver - detailed schematics.

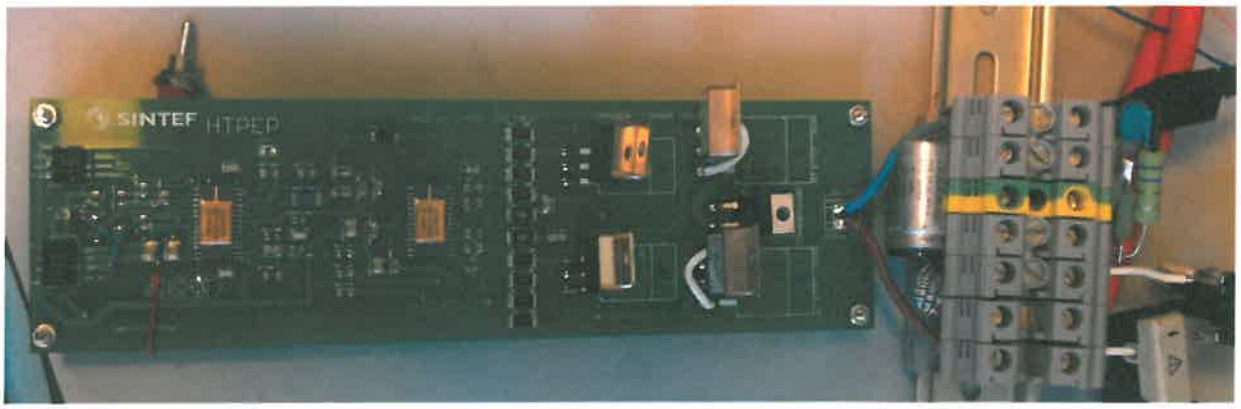


Figure 48. Picture of mounted circuit board with load and filter.

The CISSOID chipset based circuit immediately showed unexpected behaviour.

The first board made did not work at all. An ESD issue was suspected, and a second board was prepared and tested. This second board worked better but with excessive ringing when the transistors were switched on.

The circuit was tested with DC voltage up to 200 V. The rise time was an impressive 10 ns and the fall time was 60 ns (Figure 49).

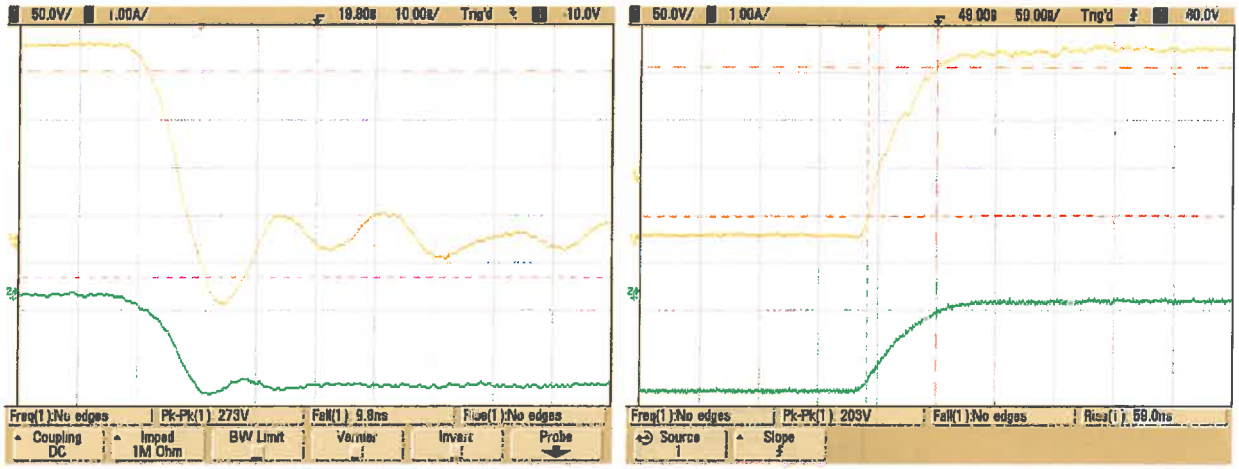


Figure 49. Turn- on was measured to 10 ns, turn off was measured to 60 ns.

When used as a half bridge, the CIDDOID parts were found to be highly self-destructible, even without a load connected. As the circuit was tested and the duty cycle increased the THEMIS or ATLAS would lock-up with a high current drawn, requiring the circuit replaced. This happened unpredictably without warning and several times (but at different circuit settings).

Other problems were also identified, even though testing periods were short due to the volatile nature of the circuit. The high side transistor was turned on parasitically when the low side turned on. This is a catastrophic condition because it gives a low impedance path from high voltage DC to ground, effectively causing a short circuit.

During testing the THEMIS chips were gradually taking more and more current for a given duty cycle, meaning that the chip was gradually failing. This was observed both using amp-meter and an IR-camera. The current drawn by THEMIS (from its 18V supply) started as 18mA but increased to more than 100mA, even in stand-by.

The fault could be related to the ATLAS chip being overloaded so CISSOID were contacted to ask how to parallel multiple ATLASes to one THEMIS, as suggested by the datasheet. The issue was not resolved with CISSOID as they could not provide any information as to how the additional ATLAS could be inserted into the circuit.

Due to the volatile nature of the CISSOID chips, their lack of support and their requirement of SINTEF signing a crippling non disclosure agreement (NDA) it was decided that an alternative circuit be devised. It has since been confirmed that CISSOID has a habit of releasing products before they are debugged, as evidenced also by the errata that came with the documentation.

The NDA, for the bare die components, turned out to be a show stopper for preparation of the base driver design. No information about the metallization system on the dies could be retained without it. As explained in the forgoing sections (2 to 0) this information is crucial to build a reliably packaged device, since substrates and interconnect technologies needs to be compatible with this metallization. Thus we were unable to plan the base driver design.

8.3.2 An alternative driver: IXYS DEIC420

We found that IXYS RF had a driver (DEIC420) specifically made for bipolar junction transistors (BJT). It was very close to the obsolete driver circuit IXYS509 recommended by TranSiC/ Fairchild. It was, however, a more powerful, offering 20 A peak current and 4 ns rise/fall times. It could have VCC levels of 8 to 30 V.

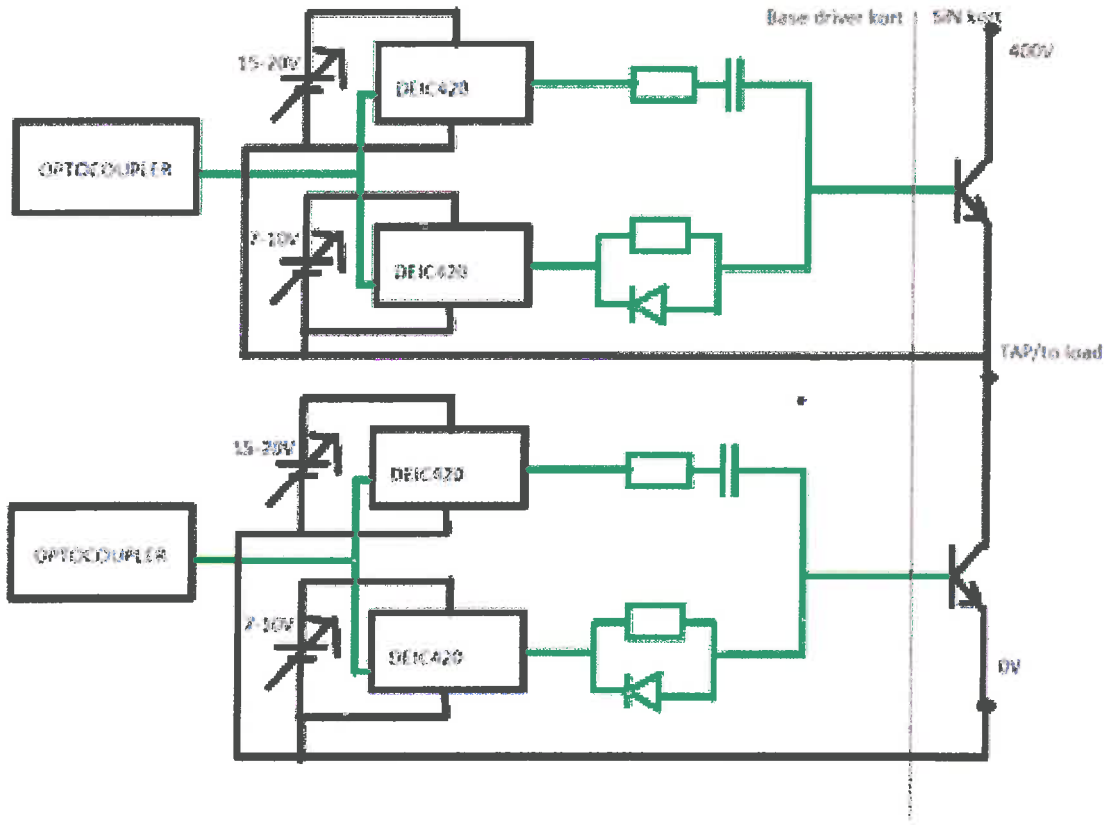


Figure 50. DOIC420 based circuit.

A half bridge driver with symmetric layout was designed and fabricated (Figure 50 and Figure 51). Furthermore, two drivers per transistors were integrated into the design: One to turn the transistor quickly on and off, and one to drive the steady-state on-period. This should give an overall power saving in the power transistors due to the lower steady-state current and faster switching.

The circuit board had 35 µm copper on all four layers, and was produced in a Rogers 4350 high temperature substrate (T_g = 280 °C and T_d = 390 °C). The base driver layout with the copper layer designs is presented in Figure 52.

The circuit seemed to drive the BJTs very well when the high voltage DC supply was off, but as soon as that supply was turned on, the high side optocoupler failed. The problem was consistent even after replacing the optocoupler with a different part. It is not uncommon for optocouplers to show such behaviour and so a more robust solution had to be found.

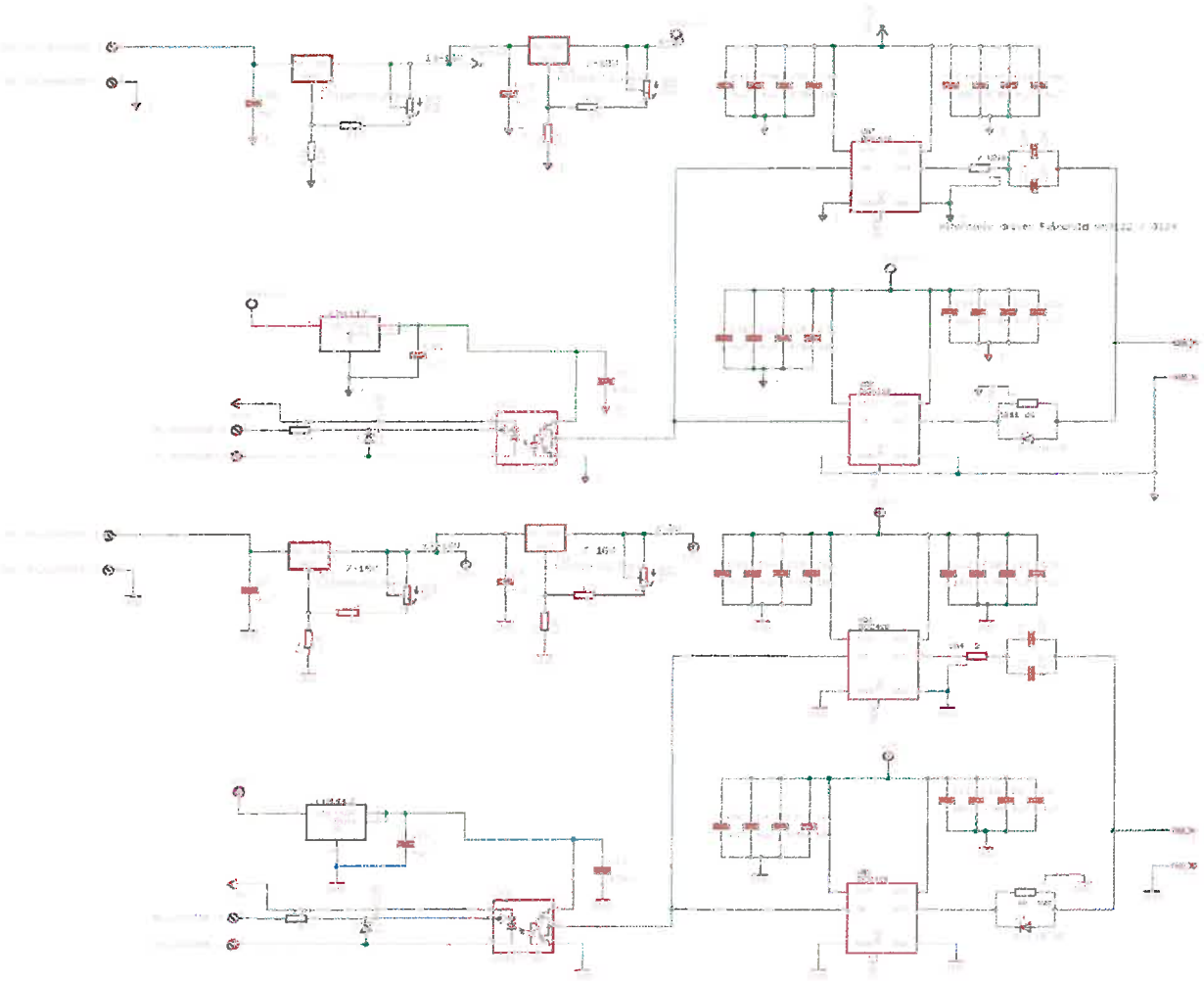


Figure 51. Detailed schematics of the DEIC420 half bridge driver.

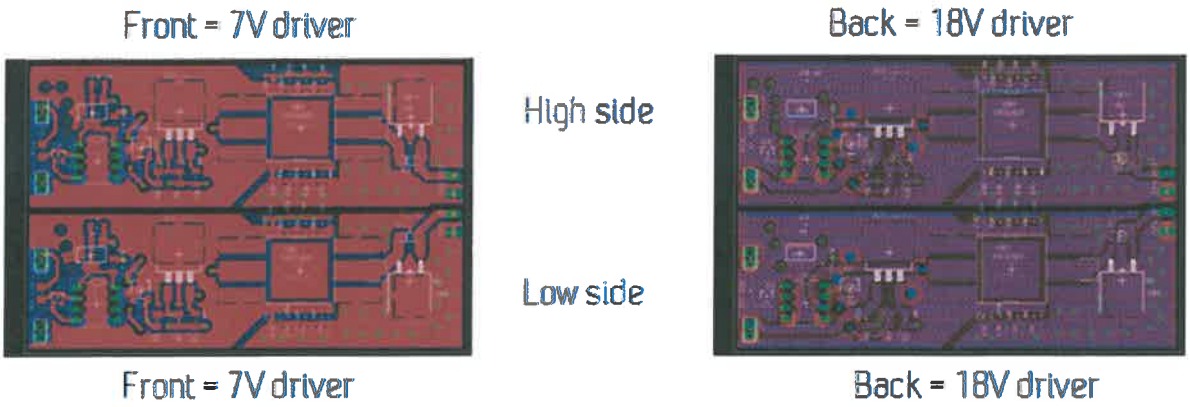


Figure 52. Base driver layout. The copper layers were symmetrical and with minimum inductance.

8.3.3 Agilent HCPL3000

It was identified that Agilent had a recently made obsolete (but still easily accessible) driver/ optocoupler that could potentially drive the BJT on its own. It was called the HCPL3000 and sported a 2 A peak drive, 0.6 A continuous pull up driver and a 1 A peak/ 500 mA continuous pull-down driver and accepted a supply voltage of 5 to 13 V. It had a propagation delay longer than ideal for our desired switching frequency of 100 kHz and the drive was weaker than wanted. Anyway, we decided to test it as a BJT driver initially, and then later insert it in place of the faulty optocoupler in the DEIC420 circuit (cf. Figure 50).

The initial tests were carried out in a full bridge topology using a non-inductive load resistor (Figure 53). This would avoid potential destructive behaviour and parasitic turn-on from having large inductances. Once the circuit was optimized the load could gradually be made more inductive.

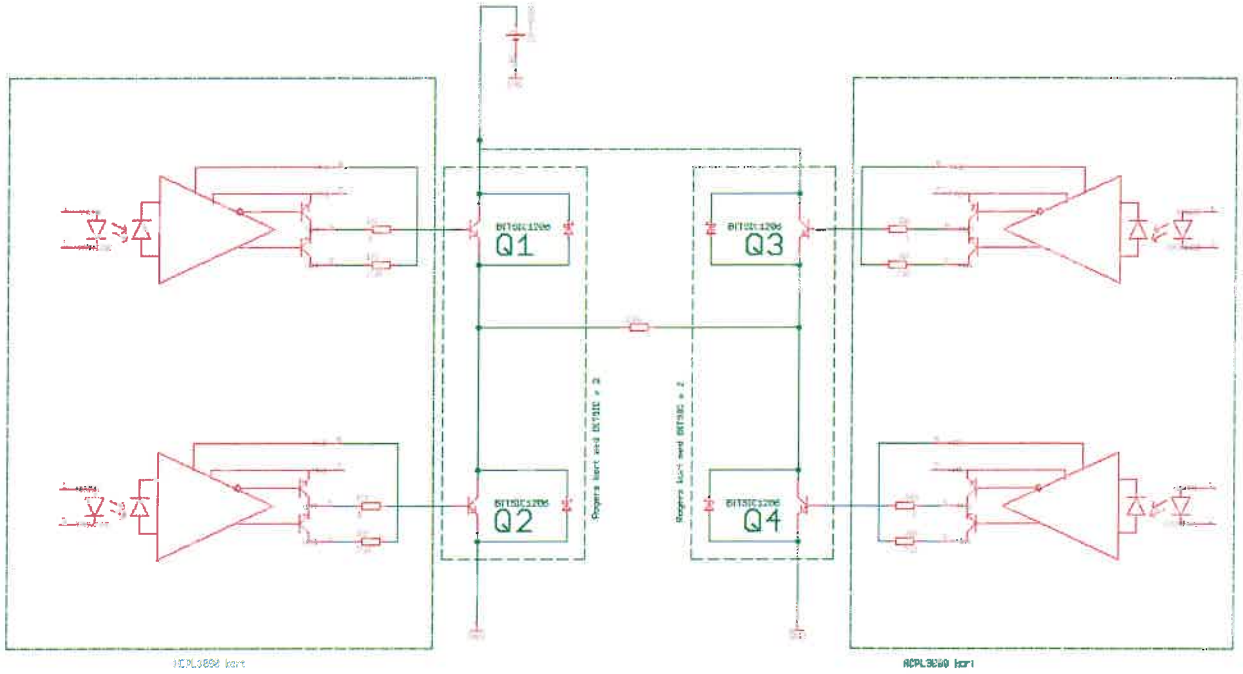


Figure 53. The HCPL3000 was tested as a full bridge, initially to drive the BJTs directly.

Q1 showed a turn on time of 76 ns and a turn off time of 370 ns. Q2 had a turn on of 91.5 ns and a turn off of 346 ns.

Although the circuit behaved like planned the switching was not very fast, as the HCPL3000 did not provide enough current to the bipolar transistors. This was not unexpected because of the limited current driving capability of the HCPL3000. Nevertheless the test showed that it was possible to test a half bridge configuration without circuit destruction and test the timing for turning on and off the various transistors.

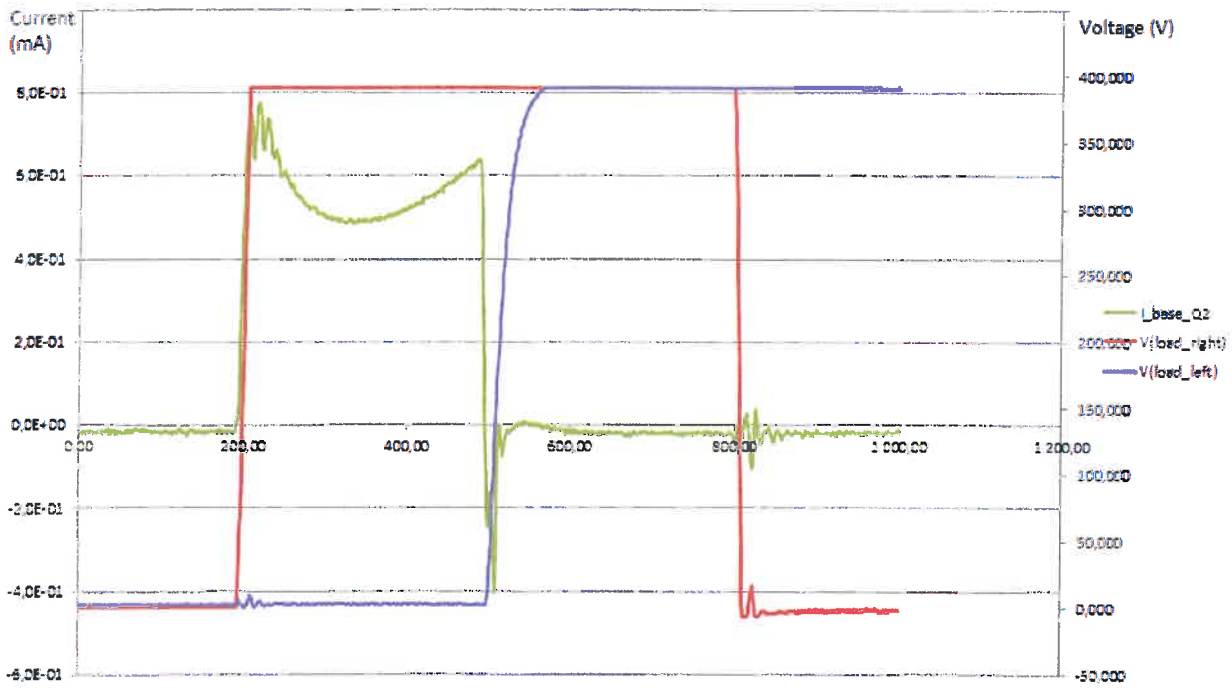


Figure 54. Q1 switching 400 V to a 100 Ω resistive load.

8.3.4 The final driver using DEIC420 with HCPL3000 optocoupler

The circuit was set up as a single low side driver due to shortage of DEIC420 chips (Figure 55).

This time the switching times were much better, with a rise time of 23 ns and a fall time of only 50 ns.

These measurements were done with no optimisation of the resistors for the peak and steady-state base current, and therefore the switching times could probably be made even shorter.

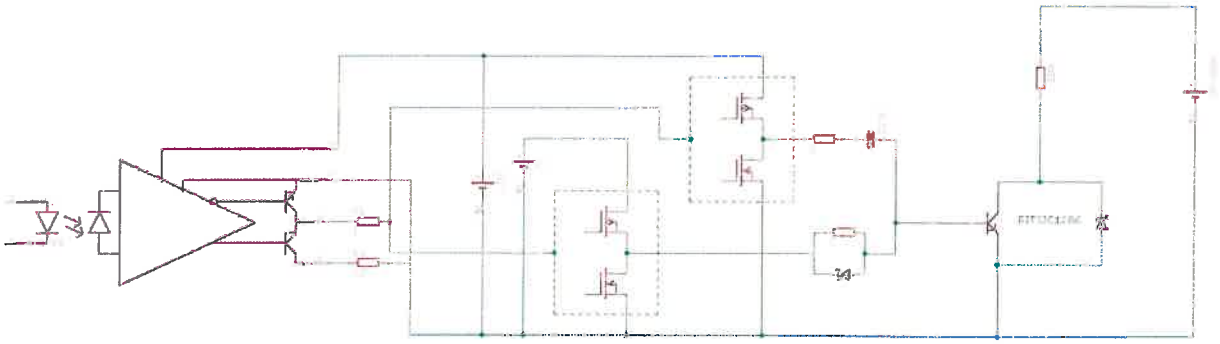


Figure 55. Using the HCPL3000 as the optocoupler to DEIC420. Cf. Q2 in Figure 53.

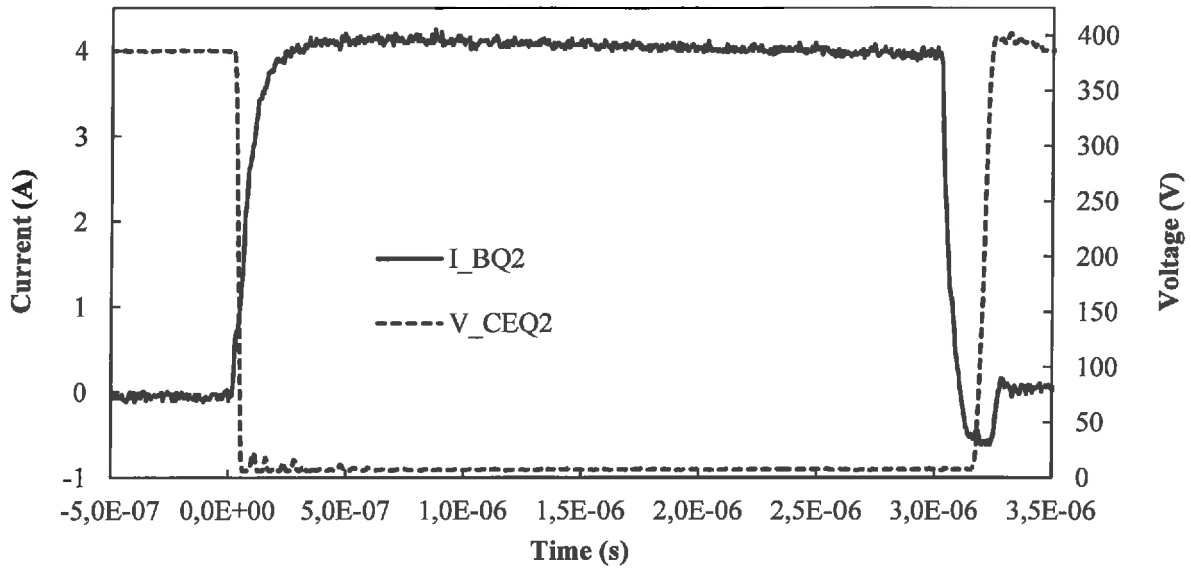


Figure 56. Characteristic switching with the DEIC420 with a HCPL3000 optocoupler. Rise time: 23 ns. Fall time: 50 ns. Q2 reefers to the low side driver in Figure 53.

We did not have a specific motor or load targeted for the case study because it was related to research and not intended for a specific product. It was estimated that a current of 4 to 6 A would be suitable and that the voltage could be in the range of 100 to 400 V.

The tests above were taken with a resistive load.

8.4 The power stage circuit board (Power module)

A schematic diagram of the output stage (power module) is shown in Figure 57. It comprises the main power switching components and was therefore of primary interest for the electronics. Here the combined effects of the need for small dimensions in order to reduce stray inductance, high power density and strong electric fields had to be traded against each other.

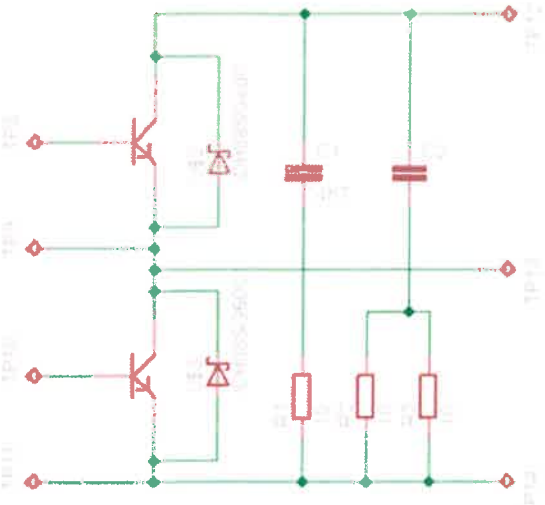


Figure 57. The power stage circuit diagram including a snubber network.

The high temperature Si_3N_4 board was given a lay out as shown in Figure 58.

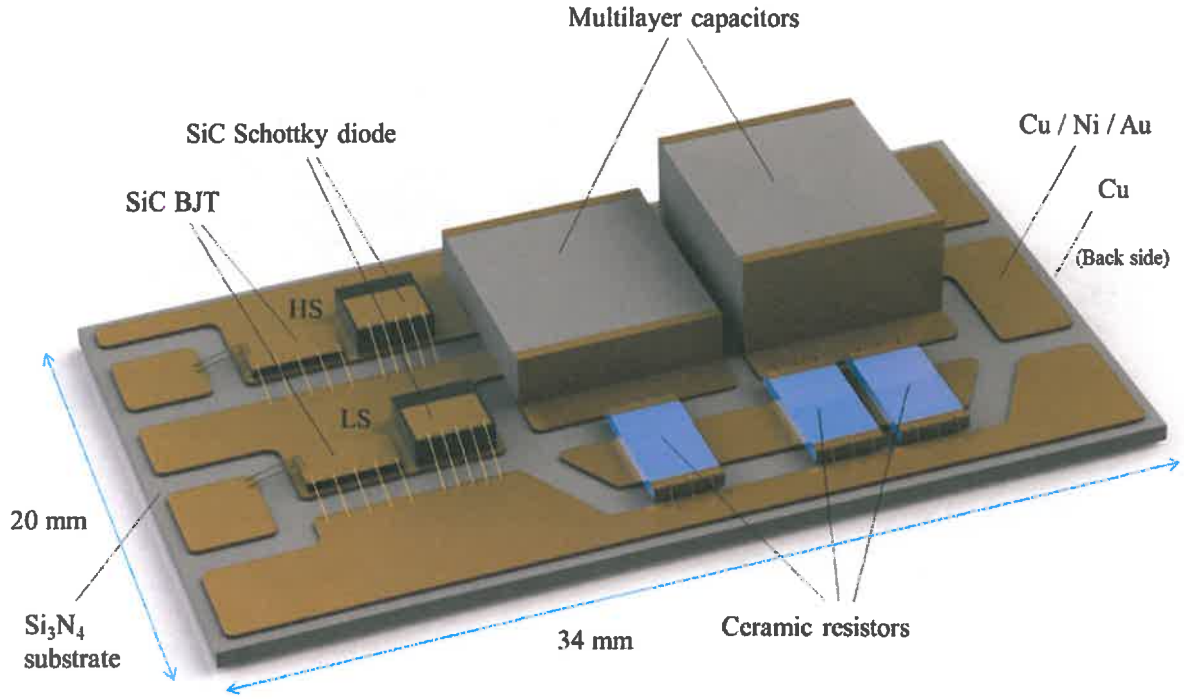


Figure 58. Silicon nitride board with bare die components. (Cf. the corresponding schematic layout in Figure 57.)

The following components were included in the power module design:

- Transistors (BJT): Fairchild (TranSiC) BitSiC 1206 1200 V 6 A SiC bipolar junction transistor
- Diodes: CNM 600 V 3 A SiC Schottky diodes
- Capacitors: TRS Technologies 110 nF and 5 nF rated to 250°C
- Resistors: Vishay Sfernice 10 Ω 110 mW

8.4.1 Power losses and temperature distribution

The power losses of the various components on the power circuit board are generally taken from simulations. The results are shown in Figure 59 (also used as input to simulations, cf. section 7). This will theoretically lead to a temperature distribution as illustrated by the finite element analysis results in section 7 and reprinted in Figure 60.

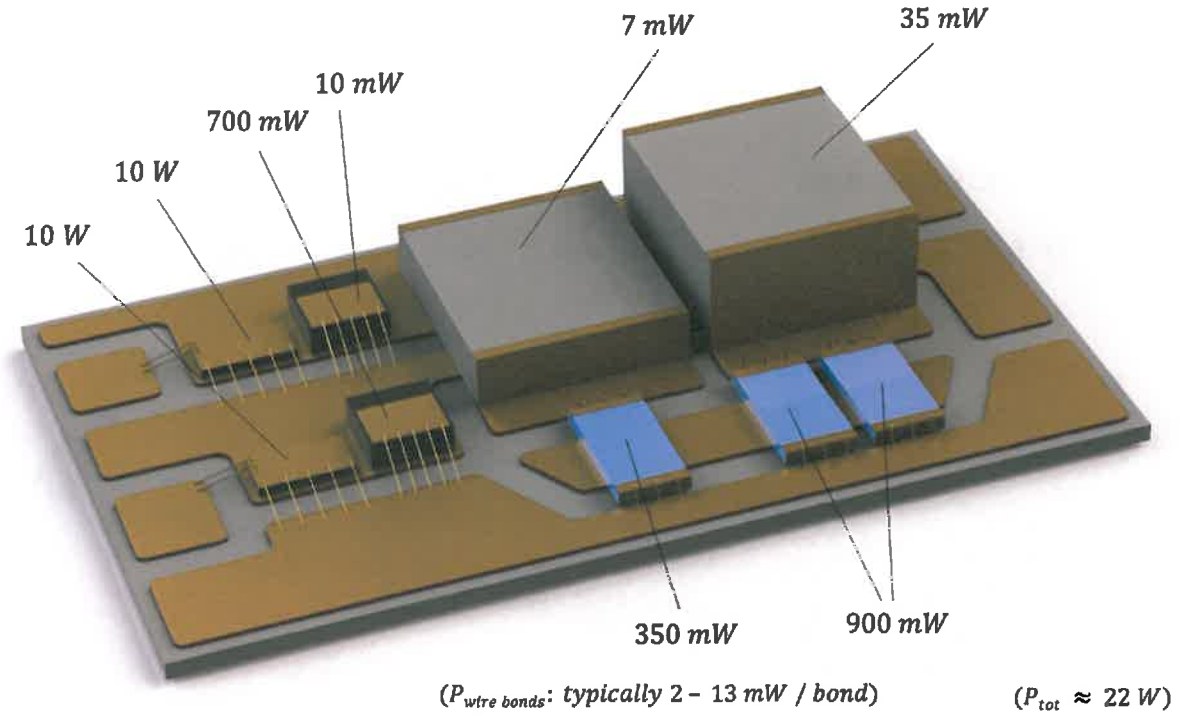


Figure 59. Power losses in the different components of the power module.

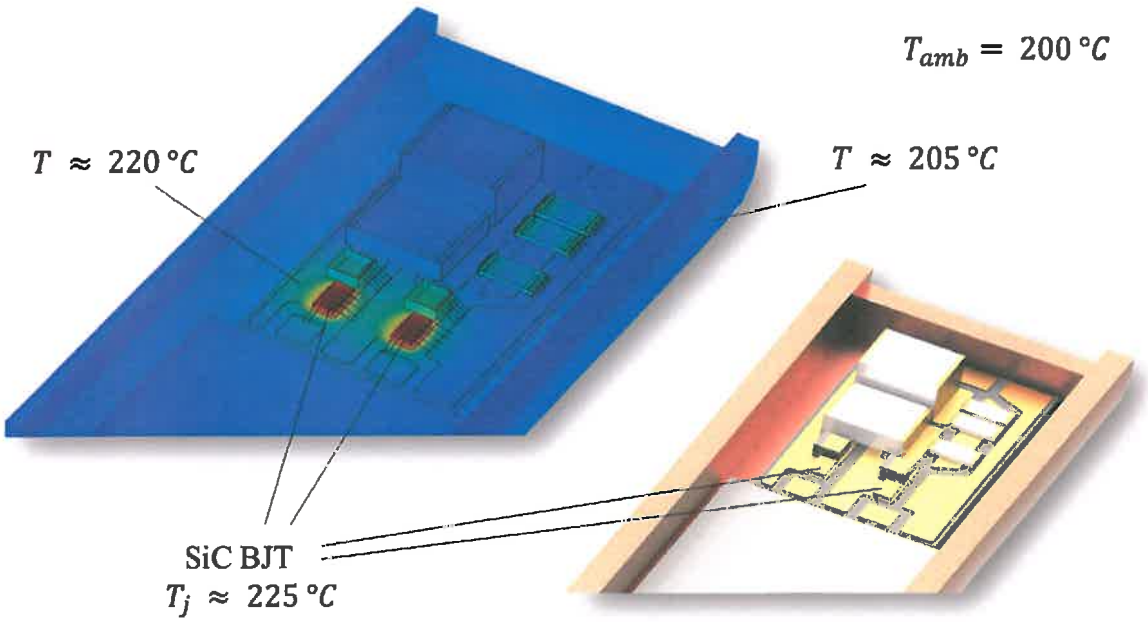


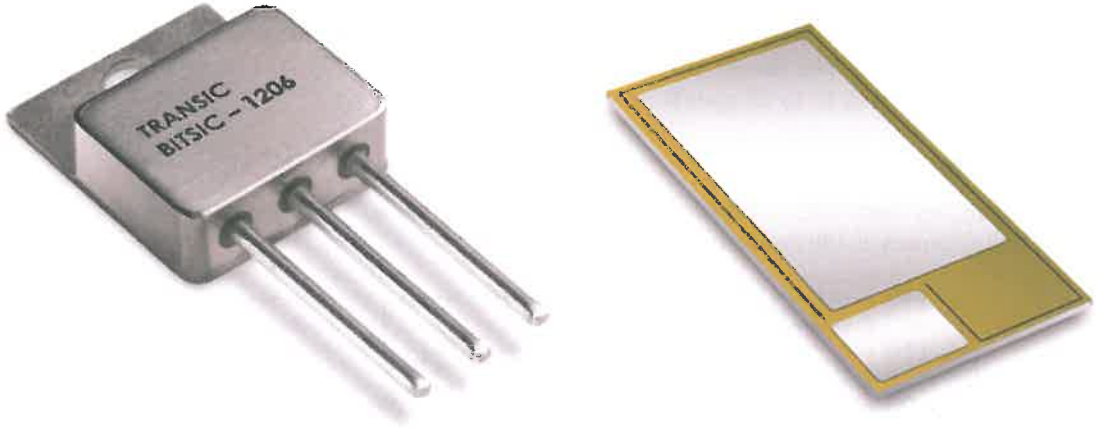
Figure 60. Temperature distribution of the power module.

8.5 Components used

Generally, the components needed for high temperature power electronics are not easily obtainable. The commercial availability is small and the specifications are often not really satisfactory. A small survey of the components used is therefore given below.

8.5.1 Transistors

The main switching elements were bipolar silicon carbide junction transistors from TranSiC/Fairchild type BitSiC 1206. They are normally delivered packaged as shown below. Two versions were available: One unit with 900 V, 20 A rating and another 1200V, 6A, illustrated in Figure 61.



(a) (b)

Figure 61. SiC bipolar junction transistor (BJT): BitSiC 1206. (a) – Photograph of metal packaged die, (b) – Illustration of a bare die with Au metallization.

For our high temperature application, bare die dummy versions of the transistors were obtained (with gold metallization in order to get a reliable bond to our Si_3N_4 substrate) for packaging experiments (Figure 62). Near the project end, sharp transistors (with the developed metallization scheme) were obtained but unfortunately no properly bonded devices could be characterized in time before project closure.

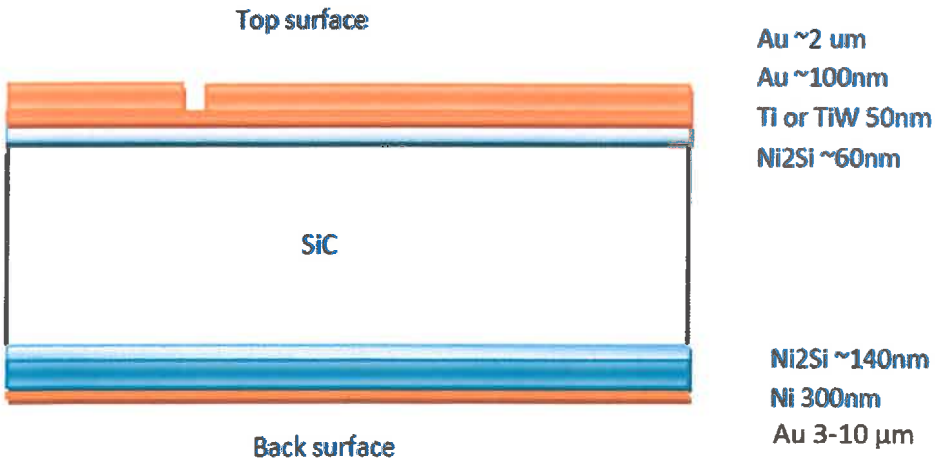


Figure 62. Developed metallization scheme for the BitSiC BJT.

8.5.2 Schottky diodes

We used SiC diodes (non commercial) from D+T Microelectrónica A.I.E. in Spain which were delivered with an appropriate gold metallization; 3 µm on topside and 0.2 µm on the backside. The diodes were rated to 500 V, 3 A and an operating temperature of 250 °C. They had a footprint of 2.9 x 2.9 mm^2 (about the same as the BitSiC transistor). Both Infineon and Cree were also contacted, but none could supply the diodes with a Au metallization.

8.5.3 Resistors

The resistors used were surface mounted types (SMD) in size 2010 (5.1 x 2.5 mm^2) supplied from Vishay (PHT series). The power rating was 100 mW at 215 °C and the maximum voltage rating was 300 V. The metallization was <1 µm gold (wire bondable) and they had a suitable coefficient of thermal expansion (CTE) 6-7 ppm/K (Al_2O_3). The maximum operation temperature was 230 °C (15000 hours). The electrical temperature coefficient was 15 to 55 ppm/K.

8.5.4 Capacitors

Multilayer capacitors from TRS Technologies in the USA were used, which have their optimal performance at elevated temperatures as illustrated in Figure 63.

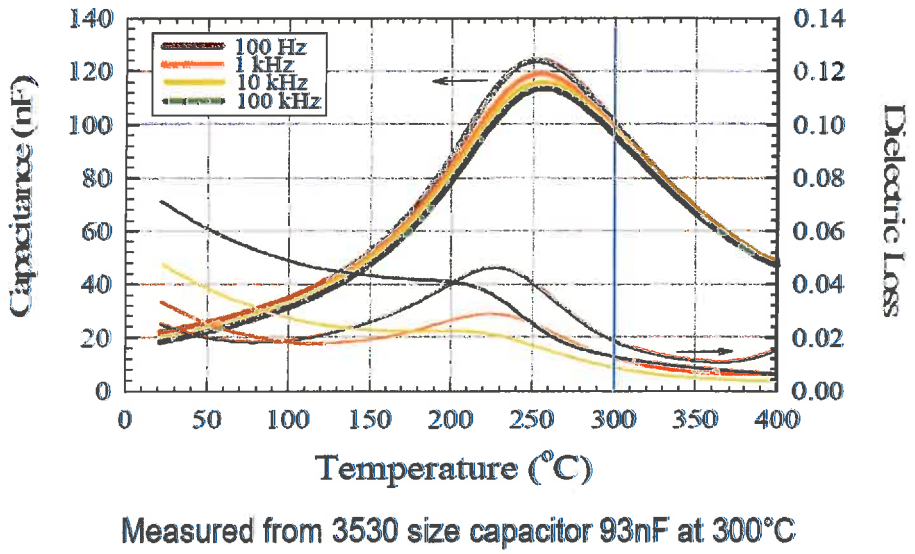


Figure 63. Thermal behaviour of TRS capacitors.

They had a maximum temperature rating of 300 °C and a voltage rating of 500 V (which was not necessary to be de-rated according to TRS). The component size was 3530 (8.9 x 7.6 mm^2) and the capacitors had a metallization of 6 to 9 µm gold.

Basic soldering tests in the lab revealed that the contact terminals were non-flat and non-parallel. Further investigation (by interferometry, WLI) showed that the terminals were very rough as well. An attempt to polish the contacts were done to prepare then for improved soldering results, e.g. with eutectic Au-Ge. The contacts still showed large peak-to-peak variations (about 50 µm) within individual contacts explaining why wetting during soldering was partial, i.e. it was hard to solder both contact terminals to the substrate.

Other high temperature capacitors suppliers investigated include: ipdia, Novacap, Kemet, CalRamic, Eurofarad and AMC.

8.5.5 Substrate

The silicon nitride (Si_3N_4) active metal brazed (AMB) ceramic substrate used (20 x 34mm^2) came from DENKA Chemicals in Japan. It had a 635 µm thick ceramic core with 150 µm Cu on both sides. It is shown in Figure 64 and described in further detail in section 0. They had a surface roughness of 3 µm and could be delivered with Ni:P (8-12%) as top metallization as an option. A schematic illustration of a cross-section of the circuit board in shown in Figure 65.

Other specifications were:

- Bending strength: >600 MPa
- Warpage: ±0.01 mm at RT
- CTE: 2-3.8 ppm/K at 250-300 °C
- Thermal conductivity: 90 W/mK at RT (only Si_3N_4) (Cu has 385 W/mK)
- Maximum board size: 60 x 60 mm^2

As mentioned in section 0, other suppliers of similar high temperature ceramic substrates are Curamik and Kyocera.

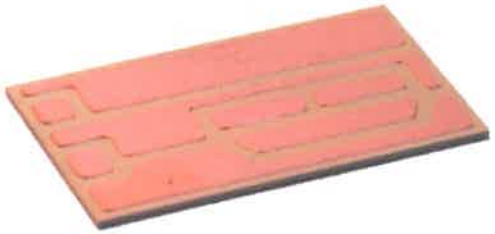


Figure 64. Fabricated Si_3N_4 substrate.

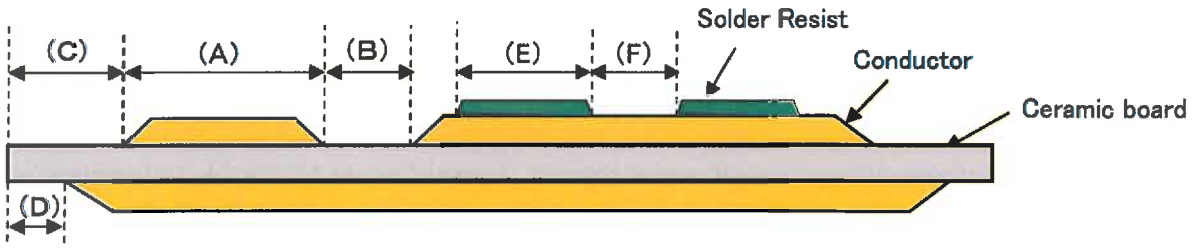


Figure 65. A schematic cross-section of the used substrate (Conductor: Cu. Ceramic board: Si_3N_4). Including typical important dimensions (A to F) and the possibility for solder resist.

8.5.6 Packaging methods for the components

Several different packaging methods were chosen for the different components of the power module. They are described in further details in the foregoing sections (0 to 7) in this report. A compilation of the chosen methods together with their corresponding electronic components to be implemented with are given in Figure 66.

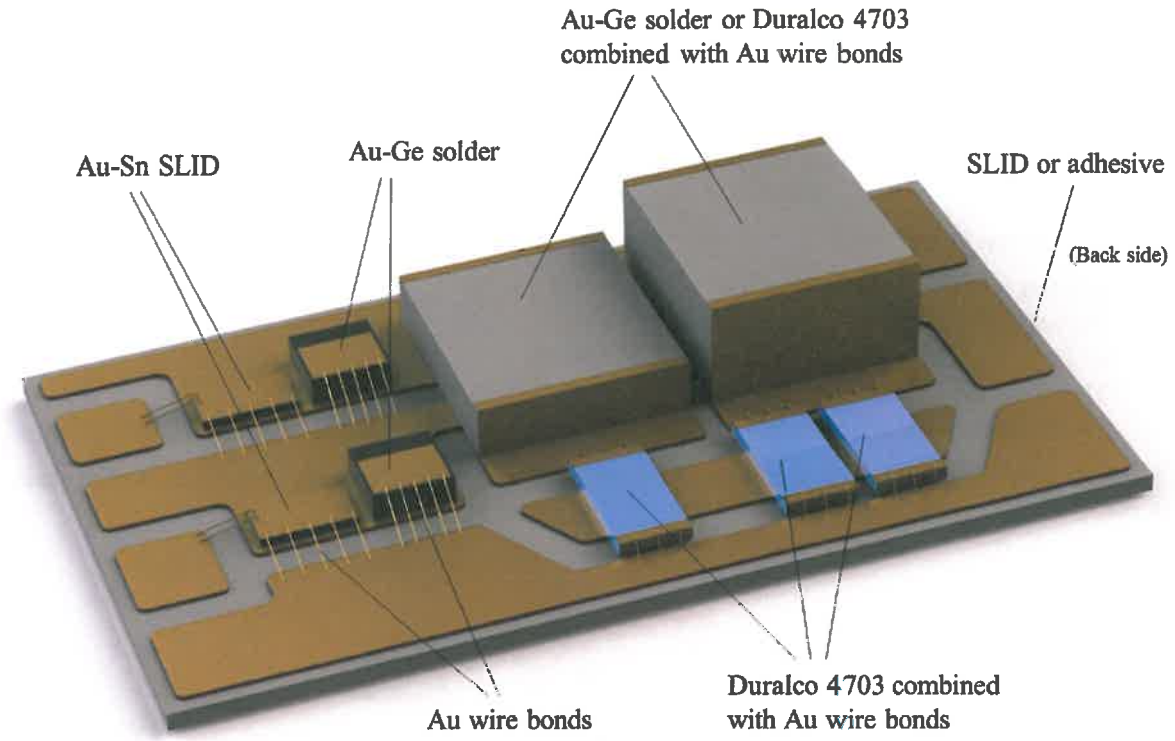


Figure 66. Chosen interconnect technologies for the power module components.

9 Acknowledgement

The authors and the active contributors to High Temperature Power Electronics Packaging (HTPEP) project would like to acknowledge the Research Council of Norway and our industry partners for their economical support and interest to the project. A special gratitude is directed to the entire consortia for their contribution to fruitful and very valuable project meetings. It has been a delight to have meetings with such a competent, interested and constructive audience and discussion partners. A special thanks to Vestfold University College for their support in supervising our research fellow as well as constructive discussions/ advises, lab disposal and scientific contributions.

A.1 Scientific equipment

Throughout the project several investments in scientific equipment was made. Since the achieved bonds were extremely strong (>170 MPa max), the project invested resources, both time and money, in a state-of-the-art shear tester (Dage 4000 Plus, Figure A 1) with a 200 kgF load cartridge. A custom made hot plate (DD6240 – Heated Adapter, Figure A 2) was also bought together with the shear tester to be able to investigate the bond strength at elevated temperatures.

A high end hot plate (PZ 28-3TD) with a uniform temperature distribution which may reach up to 600 °C and an adherent controller (PR5-3T) was purchased from Harry Gestigkeit (Figure A 3). A custom made bonder was designed and fabricated (Figure A 4) for the hot plate. The hot plate and bonder enabled bonding with tuned bond parameters (temperature, pressure and atmosphere) in normal lab environment. It was also intended to be used for high temperature storage (like a small oven) of the finalized power module while the card was characterized and during simulated operation.

Figure A 1. Dage 4000 Plus shear tester.

Figure A 2. DD6240 – Heated Adapter for Dage 4000 Plus shear tester.

Figure A 3. Programmable controller (PR5-3T) and high temperature hot plate (PZ 28-3TD) bought from Harry Gestigkeit GmbH.

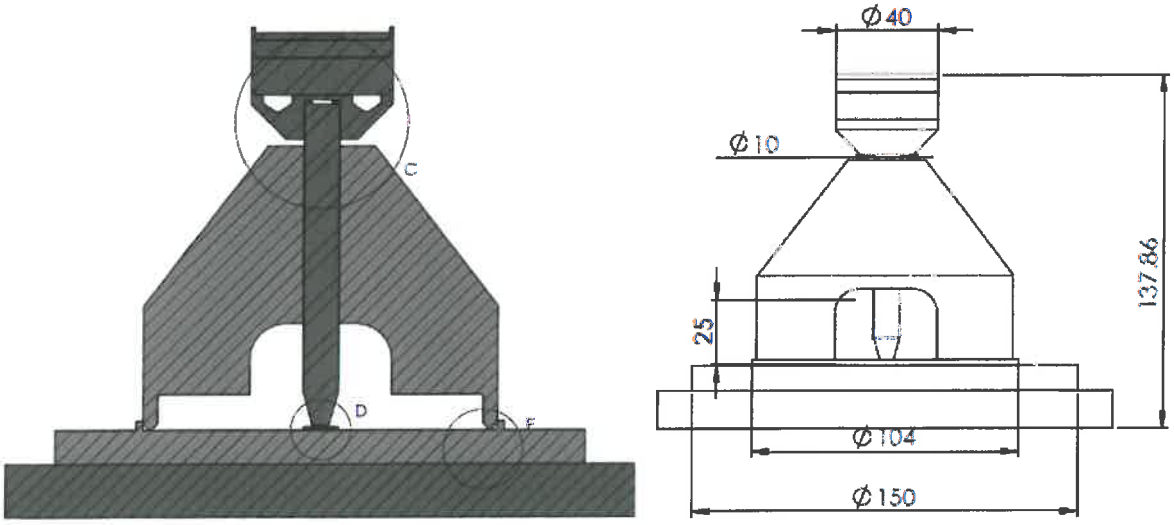


Figure A 4. The HTPEP bonder designed and fabricated in the HTPEP project. The left figure shows a cross-section of the device and the right shows typical dimensions. (A photograph of the bonder during bonding is shown in Figure 14.)

A.2 Dissertation

Journal articles

Four journal articles have been published and submitted in high level international journals. They are listed below:

2013, T. A. Tollefsen, A. Larsson, K. Aasmundtveit and O. M. Løvvik, *Effect of temperature on the die shear strength of an Au-Sn SLID bond*, Applied Physics Letters, submitted

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2013, T. A. Tollefsen, A. Larsson, M. M. V. Taklo, A. Neels, X. Maeder, K. Høydalsvik, D. W. Breiby and K. Aasmundtveit, *Au-Sn SLID bonding – A reliable HT interconnect and die attach technology*, Metallurgical and Materials Transactions B, accepted

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2012, T.A. Tollefsen, A. Larsson, O.M. Løvvik and K. Aasmundtveit, *High temperature interconnect and die attach technology – Au-Sn SLID bonding*, IEEE Trans. El. Pack. M. 2012, accepted.

2011, T.A. Tollefsen, A. Larsson, O.M. Løvvik, K. Aasmundtveit, *Au-Sn SLID bonding – Properties and Possibilities*, Metallurgical and Materials Transactions B, 10.1007/s11663-011-9609-z

International articles and posters

A total of 13 scientific articles and posters were presented on international conferences throughout the project. They are listed below:

2012, T.A. Tollefsen, M.M.V. Taklo, T. Bakke, N. Lietaer, P. Dalsjø and J. Gakkestad, *Reliability of TSVs and wafer-level bonding for a 3D integrable SOI based MEMS application*, IWLPC, San Jose, US

2012, T.A. Tollefsen, M.M.V. Taklo, K. Aasmundtveit and A. Larsson, *Reliable HT electronic packaging – Optimization of an Au-Sn SLID joint*, IEEE ESTC, Amsterdam, NL

2012, T.A. Tollefsen, A. Larsson, M.M.V. Taklo, E. Poppe. and K. Shjølberg-Henriksen, *Die shear strength as a function of bond frame geometry – Au-Au thermocompression bonding*, IEEE ESTC

2012, A. Larsson, T.A Tollefsen, *SLID bonding for power dense applications – Thermo-mechanics*, iMAPS High Temperature Electronics (HiTEC), Albuquerque, US

2012, T.A. Tollefsen, A. Larsson, K. Aasmundtveit and M. Chen, *High Temperature bonding technology for SiC devices – Au-Sn SLID*, BSAC IAB, San Francisco, US

2012, A. Larsson, T.A. Tollefsen, O. Storstrøm Barros, *SLID bonding for thermal interfaces – Thermal performance*, iMAPS 7th European Technology Workshop on Micropackaging and Thermal Management, La Rochelle, France

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2011, T.A. Tollefsen, A. Larsson, K. Aasmundtveit, *Au-Sn SLID bonding for high temperature applications*, iMAPS High Temperature Electronics Network (HiTEN), Oxford, UK

2011, T.A. Tollefsen, A. Larsson, K. Aasmundtveit, *Au-Sn bonding for harsh environments*, 2nd Annual Workshop of the Norwegian PhD Network on Nanotechnology for Microsystems (Nano-Network), Oslo, Norway

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2011, A. Larsson, T.A.T. Seip, O. Storstrøm Barros, M.M.V. Taklo, T. Fallet, *High power module packaging design for harsh environments*, iMAPS - 7th International Conference and Exhibition on Device Packaging, Scottsdale, Arizona, US

2011, A. Larsson, T.A.T. Seip, O. Storstrøm Barros, T. Fallet, *High temperature power electronics packaging*, iMAPS - 6th European Technology Workshop on Micropackaging and Thermal Management, La Rochelle, France

2010, T.A.T. Seip, A. Larsson, O.M. Løvvik, K. Aasmundtveit, *High temperature electronics packaging – Novel design, failure mechanisms and material properties*, 1st Annual Workshop of the Norwegian PhD Network on Nanotechnology for Microsystems (Nano-Network), Tønsberg, Norway

2009, R. Johannessen, A. Larsson, F. Oldervoll, T. Fallet, *High temperature power electronic packaging for oil well applications*, iMAPS High Temperature Electronics Network (HiTEN), Oxford, UK

International and national popular scientific presentations

Four popular scientific presentations were held were presented on international conferences throughout the project. They are listed below:

2012, A. Larsson, *Packaging for high temperature electronics*, (Invited talk) Commercializing micro- and nanotechnology (COMS), Tønsberg, Norway, 2012

2011, T.A. Tollefsen, A. Larsson, and K. Aasmundtveit, *High temperature bonding technology for SiC devices – Au-Sn SLID*, Invited talk at Berkley University of California, San Francisco, California, US

2011, T.A.T. Seip, A. Larsson, O.M. Løvvik, K. Aasmundtveit, *Au-Sn SLID bonding for HT applications*, Seminar at HiVe, Horten, Norway

2011, F. Oldervoll, A. Larsson, *High Temperature Electronics Packaging - HTPEP*, (Invited talk) Workshop at NTNU, Trondheim, Norway, 2011

Workshops

Two workshops were organized together with Vestfold University College and in collaboration with another research project called *Fine Pitch Interconnect of Microelectronics and Microsystems for use in Rough Environments (ReMi)*. The two half day workshops were held at Vestfold University College in Horten, Norway in 2010 and 2011. They were called *Bonding technology for rough environments* and *Electronic packaging for harsh environments* respectively.

Attention

An abstract about the HTPEP project was prepared by Truls Fallet to contribute to a national investigation performed by the research council of Norway (PETROMAKS/DEMO 2000) on Energy efficiency improvement and reduction of greenhouse gases (original title: *Energieffektivisering og reduksjon av klimagasser – En analyse av offentlig petroleumsforskning*), ISBN 978-82-12-03101-2, June 2012.

A.3 Reports and technical notes

The following technical documents were prepared during the project:

TN (000) - HTPEP Status – Technical notes.docx
TN (001) - Thermo-electrical plain bearing.pdf
TN (002) - Au thickness investigation - 2D Reduced model.docx
TN (003) - Au thickness investigation - 2D Complete model.docx
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